

# GAIA SATA DiskOnModule

## HSH40(RB0/RB4) Series

(7+15Pin Horizontal SATA DOM)



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Revision	Date	Major Changes
1.0	2009/6/16	1. Preliminary
A.0	2009/8/27	1. Formal Release

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*The information and specifications provided in this document should be used for comparative analysis and reference purposes. The content of this document is subject to change without prior notice.*

# SATA DiskOnModule

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## 1. Product Description

### 1.1 Product Overview

CoreSolid Storage's SATA DiskOnModule (DOM) is the storage device based on NAND flash memory technology. This product complies Serial ATA standard interface and is suitable for data storage media and code storage device for embedded system and boot disk. By using **SATA DiskOnModule**, it is possible to operate good performance for the systems, which have SATA interface.

With small form factor, the applicable appliance can add or install SATA storage device on its Mother Board or Complete set.

#### Application Fields:

- Industrial PC and Thin Client
- Game and Telecommunication Machine
- Ticketing, Examining, testing machine
- Army, Health and Production Equipment and Machine
- Other machines and Equipments with Serial ATA 3.0Gb/s Interface.

### 1.2 Product Features

- Small form factor with Serial ATA Standard Interface connector
- Memory Capacities: 128MB ~ 16GB (normal temperature), 128MB ~ 8GB (wide temperature)
- High performance and reliability
- Noiseless and stable installation to system
- Operating voltage only 5V operation
- Standard Serial ATA Interface
- Operating as Boot Disk
- Code Storage Device for Embedded Operating System

### 1.3 System Requirement

- The Host system which is connected to SATA DiskOnModule should meet system requirements at minimum;

#### 1.3.1 Power Requirement

- Voltage: DC +5V  $\pm$  5%

#### 1.3.2 Operating System

- Windows 2000/XP/Vista
- Linux
- DOS
- WinXP Embedded
- WinCE

#### 1.3.3 Interface

- Standard SATA 3.0Gb/s Interface

# SATA DiskOnModule

## 2. Specification

### 2.1 Physical Specifications

#### 2.1.1 Overlook

The overlook views of 7+15Pin Horizontal SATA DiskOnModule, HSH40(RB0/RB4), are illustrated in Figure 1.

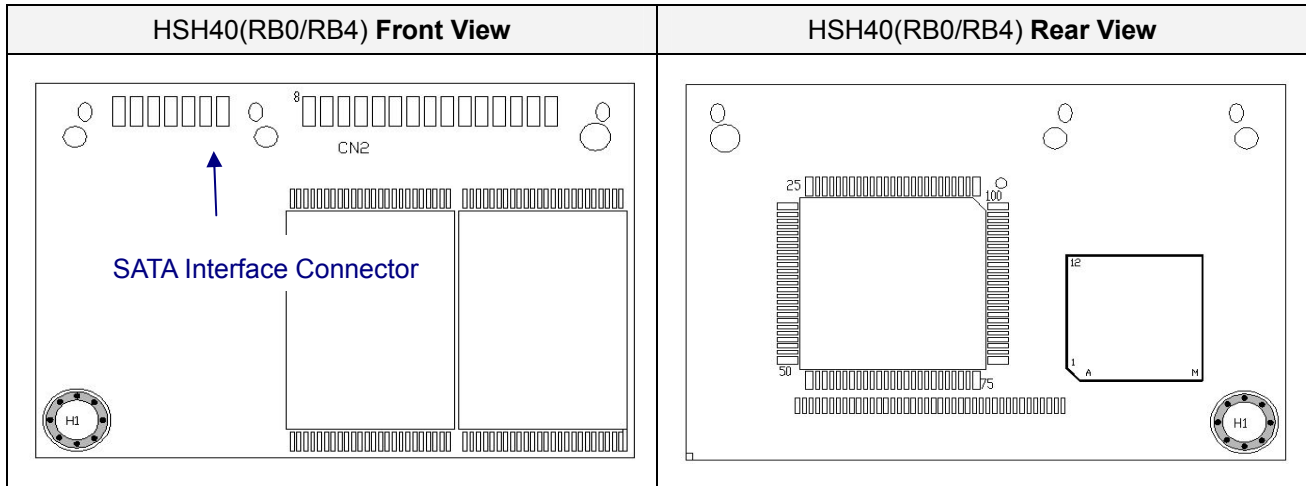


Figure 1: 7+15Pin Horizontal SATA DiskOnModule Overlook Diagram

#### 2.1.2 Dimension

The Dimensions of 7+15Pin Horizontal SATA DiskOnModule are illustrated in Figure 2 and described in Table 1.

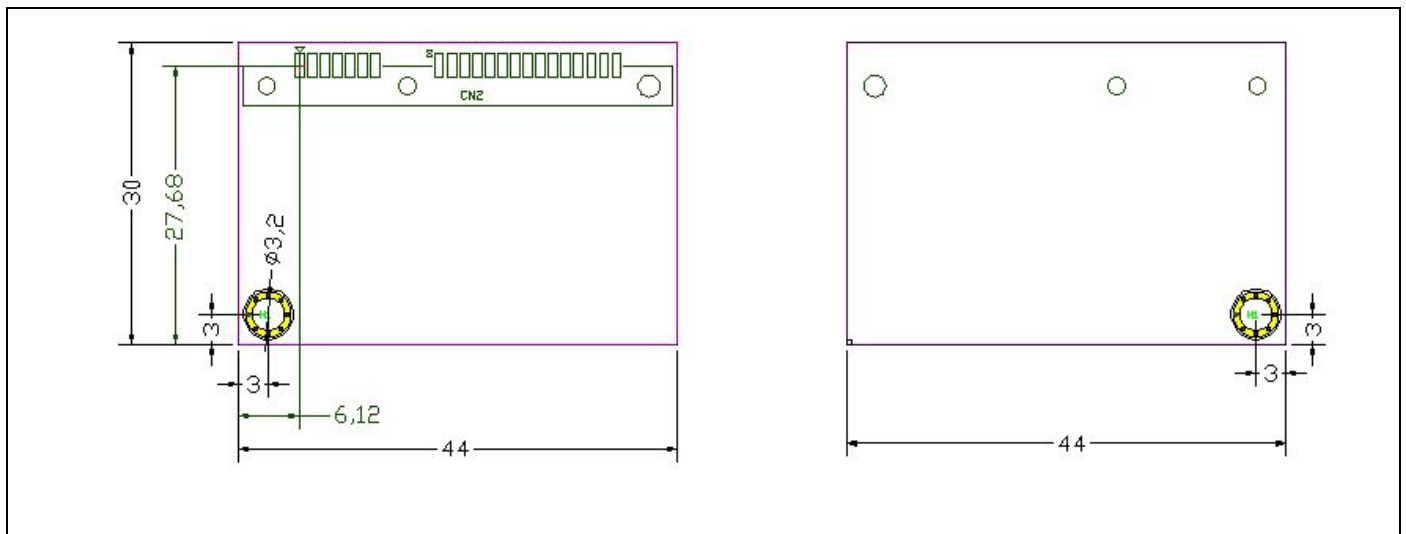


Figure 2: 7+15Pin Horizontal SATA DOM Dimensions

Table 1: 7+15Pin Horizontal SATA DiskOnModule Physical Dimension

Height	30.0 ± 0.15 mm
Width	44.0 ± 0.15 mm
Thickness (Connector)	10.75 ± 0.5mm

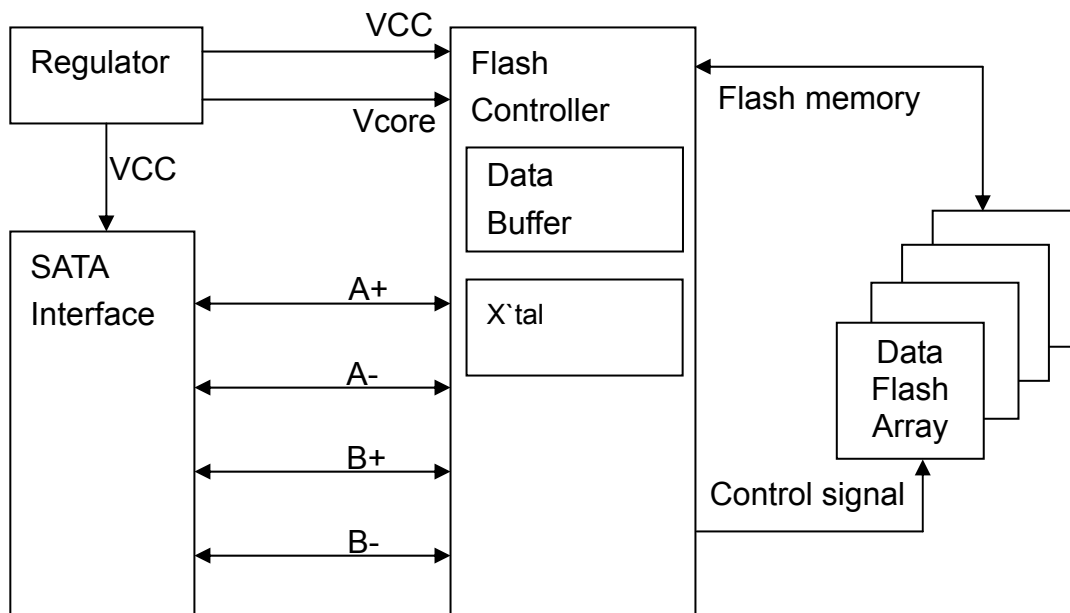
#### 2.1.3 Weight

- Weight: < 8.4g

## 2.2 Electronic Specifications

### 2.2.1 Product Definition

SATA DiskOnModule is designed to operate and work as Data or Code Storage device by NAND Flash Memory and its Controller through Standard Serial ATA 3.0Gb/s Interface to Host Systems.



**Figure 3: SATA DiskOnModule Block Diagram**

### 2.2.2 Operating Voltage

- Voltage DC +5V  $\pm$  5%

### 2.2.3 Capacity and Block Size information

- Capacity: 128MB ~ 16GB (normal temperature), 128MB ~ 8GB (wide temperature)
- Sector Size: 512Bytes

### 2.2.4 Power Consumption

- DC Information
  - Read: <230mA
  - Write: <270mA
  - Stand-by: <120mA

※ Testing Platform;

Mother-Board: ASUS P5GC-FX, CPU: Core2Dual 1.60G, Chipset: Intel 945G+ICH7, Main Memory: DDR2-400 2GB  
Operating System: WinXP.

## SATA DiskOnModule

### 2.3 Performance Specifications

#### 2.3.1 Modes

- Serial ATA 3.0Gb/s

#### 2.3.2 Access Time

- SATA DiskOnModule's maximum access time is about 0.3msec.

#### ※ Testing Platform

Testing S/W: HD Tune 2.53, Testing OS: WinXP

Mother-Board: ASUS P5GC-FX, CPU: Core2Dual 1.60G, Chipset: Intel 945G+ICH7, Main Memory: DDR2-400 2GB

Testing base: Time required Between Host to Device

#### 2.3.3 Seek Time

- SATA DiskOnModule has no seek time by being based on Flash Memory technology.

#### 2.3.4 Mount Time

The Mount Time for initializing and mounting SATA DiskOnModule is different by depending on Operating System and testing Platform.

#### 2.3.5 Data Transfer Time

- Sequential Read: up to 20 MB/sec for Single Mode, or 40MB/sec for Dual mode
- Sequential Write: up to 10 MB/sec for Single Mode, or 20MB/sec for Dual mode

#### ※ Test Platform: Average Value based on Serial ATA 3.0Gb/s interface

Mother-Board: ASUS P5GC-FX, CPU: Core2Dual 1.60G, Chipset: Intel 945G+ICH7, Main Memory: DDR2-400 2GB

Testing Software: HD Bench 3.4 Testing OS: Windows XP

**Notice:** The value is various bases on the testing platform.

#### 2.3.6 Data Retention

- 10years without requiring power support

**Notice:** The Value of Data Retention is various bases on the type and manufacturer of Flash Memory

#### 2.3.7 Wear-leveling

- Static Wear-Leveling for same level of Write/Erase Cycle

#### 2.3.8 Bad Block Management

- The Bad Blocks of Flash Memory will be replaced into new ones by controller.

### 2.4 Environmental Specifications

#### 2.4.1 Temperature

- Operating Temperature: 0°C to +70°C, Storage Temperature: -40°C to +85°C.
- Operating Temperature: -40°C to +85°C, Non Operating Temperature: -55°C to +90°C (Wide temperature type)

#### 2.4.2 Humidity

- Operating Humidity (30°C Max. Wet Bulb Temp): 10% to 95%.
- Non-Operating Humidity (30°C Max. Wet Bulb Temp): 10% to 95% (with no condensation relative humidity).

#### 2.4.3 Bare Drop test

- Test Conditions: 75cm height
- Test Orientation: (Free fell) Front/Rear/Right/Left/Top/Bottom side
- Test Result: Pass

## 2.4.4 Vibration

- Random Vibration (Operation): Test Specification

Frequency(Hz)	PSD(G <sup>2</sup> /Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.01	6Grms	30min per axis (X,Y,Z)
100	0.08		
500	0.08		

- Sine Vibration (Non-Operation): Test Specification

Frequency(Hz)	PSD(G <sup>2</sup> /Hz)	Acceleration (G)	Dwell Time (Min)
10	0.01	15G	30min per axis (X,Y,Z)
100	0.04		
500	0.04		
2000	0.004		

## 2.5 Reliability Specifications

### 2.5.1 ECC/EDC (Error Correction Code/Error Detection Code)

- Built-in Reed Solomon 4symbol/512 bytes

### 2.5.2 MTTF (Mean Time To Failure)

- 2,000,000hours

**Notice:** The Value of MTTF is based on the specific access size, access period, and type and manufacturer of Flash Memory.

### 2.5.3 Power Cycle

- The Power Cycling is tested to 5000 loops. => "Pass"

## 2.6 Compliance Specifications

- CE

- FCC

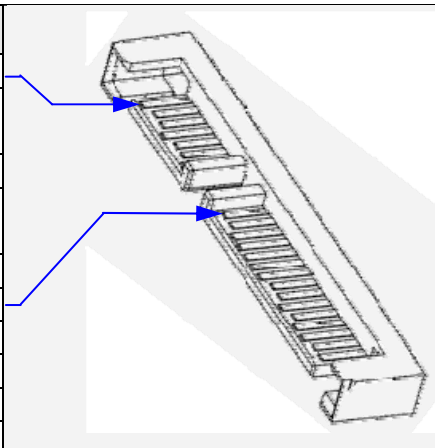
### 3. Function

#### 3.1 Pin Signal Assignment

The signals assigned for Serial ATA applications are described in Table 2

**Table 2: Serial ATA connector pin definitions**

Segment	Pin No	Function	Definition
Signal	S1	Gnd	Differential signal pair A from Phy
	S2	A+	
	S3	A-	Differential signal pair B from Phy
	S4	Gnd	
	S5	B-	Differential signal pair B from Phy
	S6	B+	
	S7	Gnd	
Power	P8~P10	3.3V	Voltage
	P11~P13	GND	
	P14~P16	5V	Voltage
	P17~P19	GND	
	P20~P22	NC	



**Notice:** All pins are a 1.27 mm (0.050") pitch.

**Figure 4: SATA Signal Connector**

#### 3.2 DiskOnModule Capacity and Cylinder, Head, Sector

The table 3 show various capacities available for HSH40 series, if your platform does not support auto-detection function or HSH40 series is not identified, we advice can following below Cylinders, Heads, Sectors number to setting your platform.

**Table 3: DiskOnModule Capacity and Cylinder, Head, Sector**

Unformatted Disk Capacity	No. of Cylinders	No. of Heads	No. of Sectors	Disk Total Sector
128MB	994	8	32	254,464
256MB	974	16	32	498,688
512MB	1,012	16	63	1,020,096
1GB	1,984	16	63	1,999,872
2GB	3,980	16	63	4,011,840
4GB	7,970	16	63	8,033,760
8GB	15,945	16	63	16,072,560
The following capacity are in LBA mode				
16GB	16,383	16	63	32,165,280

#### 3.3 Support ATA Commands

- ATA Command Set
  - ATA Command Set summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

**Table 4: ATA Command Set**

No	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
2	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
3	Execute Drive Diagnostic	90h	-	-	-	-	D	-
4	Flush Cache	E7h	-	-	-	-	D	-

No	COMMAND	Code	FR	SC	SN	CY	DH	LBA
5	Format Track	50h	-	Y	-	Y	Y	Y
6	Identify Device	ECh	-	-	-	-	D	-
7	Identify Device DMA	EEh	-	-	-	-	D	-
8	Idle	E3h or 97h	-	Y	-	-	D	-
9	Idle Immediate	E1h or 95h	-	-	-	-	D	-
10	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
11	Media Lock	DEh	-	-	-	-	D	-
12	Media Unlock	DFh	-	-	-	-	D	-
13	NOP	00h	-	-	-	-	D	-
14	Read Buffer	E4h	-	-	-	-	D	-
15	Read DMA	C8h	-	Y	Y	Y	Y	Y
16	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
17	Read Multiple	C4h	-	Y	Y	Y	Y	Y
18	Read Native Max Address	F8h	-	-	-	-	D	-
19	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
20	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
21	Recalibrate	1Xh	-	-	-	-	D	-
22	Request Sense	03h	-	-	-	-	D	-
23	Seek	7Xh	-	-	Y	Y	Y	Y
24	Set Features	EFh	Y	-	-	-	D	-
25	Set Max Address	F9h	-	Y	Y	Y	Y	Y
26	Set Multiple Mode	C6h	-	Y	-	-	D	-
27	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
28	SMART	B0h	Y	Y	-	Y	Y	-
29	Standby	E2h or 96h	-	-	-	-	D	-
30	Standby Immediate	E0h or 94h	-	-	-	-	D	-
31	Translate Sector	87h	-	Y	Y	Y	Y	Y
32	Write Buffer	E8h	-	-	-	-	D	-
33	Write DMA	CAh	-	Y	Y	Y	Y	Y
34	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
35	Write Multiple	C5h	-	Y	Y	Y	Y	Y
36	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
37	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
38	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
39	Write Verify	3Ch	-	Y	Y	Y	Y	Y

## Definitions:

FR = Features Register

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Registers

DH = Device/Drive/Head Register

LBA = Logical Block Address Mode Supported (see command descriptions for use).

Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the device and head parameters are used.

D - Only the device parameter is valid and not the head parameter;

C - The register contains command specific data (see command descriptions for use).

**(1) Check Power Mode - 98h or E5h**

Bit ->	7	6	5	4	3	2	1	0
Command	98h or E5h							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Check Power Mode**

This command checks the power mode.

If the device is in, going to, or recovering from the sleep mode, the device sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the device is in Idle mode, the device sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

**(2) Erase Sector(s) - C0h**

Bit ->	7	6	5	4	3	2	1	0
Command	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)					Cylinder High (LBA 23-16)			
Cyl Low (4)					Cylinder Low (LBA 15-8)			
Sec Num (3)					Sector Number (LBA 7-0)			
Sec Cnt (2)					Sector Count			
Feature (1)					X			

**Erase Sector**

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

**(3) Execute Drive Diagnostic - 90h**

Bit ->	7	6	5	4	3	2	1	0
Command	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Execute Drive Diagnostic**

This command performs the internal diagnostic tests implemented by the device.

When the diagnostic command is issued, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in Table 5: Diagnostic Codes are returned in the Error Register at the end of the command.

**Table 5: Diagnostic Codes**

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

**(4) Flush Cache – E7h**

Bit ->	7	6	5	4	3	2	1	0	
Command	E7h								
C/D/H (6)	X	X	X	Drive	X				
Cyl High (5)					X				
Cyl Low (4)					X				
Sec Num (3)					X				
Sec Cnt (2)					X				
Feature (1)					X				

**Flush Cache**

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the Flash memory. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

**(5) Format Track - 50h**

Bit ->	7	6	5	4	3	2	1	0
Command	50h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)					Cylinder High (LBA 23-16)			
Cyl Low (4)					Cylinder Low (LBA 15-8)			
Sec Num (3)					X (LBA 7-0)			
Sec Cnt (2)					Count (LBA mode only)			
Feature (1)					X			

**Format Track**

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the device expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the device. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

## (6) Identify Device – ECh

Bit ->	7	6	5	4	3	2	1	0
Command	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Identify Device**

The Identify Device command enables the host to receive parameter information from the device. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 6. All reserved bits or words are zero. Hosts should not depend on obsolete words in Identify Device containing 0. Table 6 specifies each field in the data returned by the Identify Device Command. In Table 6, X indicates a numeric nibble value specific to the device and aaaa indicates an ASCII string specific to the particular drive.

**Table 6: Identify Device Information**

Word Address	Default Value	Total Bytes	Data Field Type Information
0	0XXX	2	General configuration – Bit Significant with ATA definitions.
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Reserved for vendor
5	0200h	2	Reserved for vendor
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Reserved for assignment by the CFA
9	0000h	2	Reserved
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0002h	2	Reserved for vendor
21	000Xh	2	Reserved for vendor
22	0004h	2	Reserved for vendor
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	800Xh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0F00h	2	Capabilities: DMA, LBA, IORDY supported
50	0000h	2	Capabilities: Others, Fixed
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	Reserved
53	0007h	2	Data Fields 54 to 58, 64 to 70 and 88 are valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	010Xh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode

Word Address	Default Value	Total Bytes	Data Field Type Information
62	0000h	2	Reserved
63	0X0Xh	2	Multiword DMA transfer.
64	0003h	2	Advanced PIO modes 3 and 4 supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word.
66	0078h	2	Recommended Multiword DMA transfer cycle time.
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80	0020h	2	Major version number, ATA-5 support
81	0000h	2	Minor version number, not reported
82	7409h	2	Features/command sets supported (NOP, SMART,...)
83	5004h	2	Features/command sets supported (Flush Cache, ...)
84	4000h	2	Features/command sets supported (extension)
85	740Xh	2	Features/command sets enabled (NOP, SMART,...)
86	X004h	2	Features/command sets enabled (Flush Cache, ...)
87	4000h	2	Features/command sets enabled (extension)
88	XXXXh	2	Ultra DMA Mode Supported and Selected
89-92	0000h	8	Reserved
93	XXXXh	2	Hardware Reset result
94-129	0000h	72	Reserved
130-152	XXXXh	8	Reserved for vendor
153-159	0000h	12	Reserved
160	A064h	2	Power requirement description
161-175	XXXXh	2	Reserved for assignment by the CFA
176-254	0000h	180	Reserved
255	XXA5h	2	Integrity Word

### Word 0: General Configuration

This field indicates the general characteristics of the device.

Bit 15-12: Configuration Flag: It is fixed as 0 to represent it is an ATA device.

Bits 11-8: Retired. These bits have retired ATA bit definitions. It is recommended that the value of these bits be either the preferred value of 0h or the value of 4h that preserves the corresponding bits to one or zero.

Bit 7: Removable Media Device If Bit 7 is set to 1, the device contains media that can be removed during device operation. If Bit 7 is set to 0, the device contains non-removable media.

Bit 6: Not Removable Controller and/or Device

**Alert!** This bit will be considered for obsolescence in a future revision of this standard.

If Bit 6 is set to 1, the Device is intended to be nonremovable during operation. If Bit 6 is set to 0, the Device is intended to be removable during operation.

Bits 5-0: Retired/Reserved

**Alert!** Bit 2 will be considered for definition in a future revision of this standard and shall be 0 at this time.

Bits 5-1 have retired ATA bit definitions.

Bit 2 shall be 0.

Bit 0 is reserved and shall be 0.

## Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

## Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

## Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

## Words 10-19: Serial Number

This field contains the serial number for this device and is right justified and padded with spaces (20h).

## Words 20: Buffer type

This field contains the buffer type of the device. It is set by default.

**Alert!** *This word is considered for obsolescence in a future revision of this standard.*

## Words 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

## Words 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

## Word 47: Read/Write Multiple Sector Count

Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h. Bits 7-0 of this word define the maximum number of sectors per block that the device supports for Read/Write Multiple commands.

## Word 49: Capabilities

Bit 13: Standby Timer

If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command

If bit 13 is set to 0 then the Standby timer operation is defined by the vendor.

Bit 11: IORDY Supported

If bit 11 is set to 1 then this device supports IORDY operation.

If bit 11 is set to 0 then this device may support IORDY operation.

Bit 10: IORDY may be disabled

Bit 10 shall be set to 0, indicating that IORDY may not be disabled.

Bit 9: LBA supported

Bit 9 shall be set to 1, indicating that this device supports LBA mode addressing. Devices shall support LBA addressing.

Bit 8: DMA Supported

If bit 8 is set to 1 then Read DMA and Write DMA commands are supported.

Bit 8 shall be set to 0. Read/Write DMA commands are not currently permitted on CF devices.

### **Word 51: PIO Data Transfer Cycle Timing Mode**

The PIO transfer timing for each device falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.

### **Word 53: Translation Parameters Valid**

Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any device that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

### **Words 54-56: Current Number of Cylinders, Heads, Sectors/Track**

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

### **Words 57-58: Current Capacity**

This field contains the product of the current cylinders times heads times sectors.

### **Word 59: Multiple Sector Setting**

Bits 15-9 are reserved and shall be set to 0.

Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid.

Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands.

### **Words 60-61: Total Sectors Addressable in LBA Mode**

This field contains the total number of user addressable sectors for the device in LBA mode only.

### **Word 63: Multiword DMA transfer**

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the device to indicate the multiword DMA mode which is currently selected. Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected. Selection of Multiword DMA modes 3 and above are specific to device are reported in word 163 as described in Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data

transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the Multiword DMA modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the device supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the device supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the device supports Multiword DMA modes 2, 1 and 0.

Support for Multiword DMA modes 3 and above are specific to device are reported in Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

### **Word 64: Advanced PIO transfer modes supported**

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the advanced PIO modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the device supports PIO mode 3. Bit 1, if set to one, indicates that the device supports PIO mode 4.

Support for PIO modes 5 and above are specific to device are reported in word 163 as described in Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

### **Word 65: Minimum Multiword DMA transfer cycle time**

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, and the device guarantees data integrity during the transfer.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all device supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Device shall return a value of zero in this field.

### **Word 66: Recommended Multiword DMA transfer cycle time**

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the device will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all device supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Device shall return a value of zero in this field.

### **Word 67: Minimum PIO transfer cycle time without flow control**

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the

host, the device guarantees data integrity during the transfer without utilization of flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

### **Word 68: Minimum PIO transfer cycle time with IORDY**

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the device.

If bit 1 of word 53 is set to one because a device supports a field in words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

### **Words 82-84: Features/command sets supported**

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by device prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.

If bit 1 of word 82 is set to one, the Security Mode feature set is supported.

Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.

If bit 5 of word 82 is set to one, write cache is supported.

If bit 6 of word 82 is set to one, look-ahead is supported.

Bit 7 of word 82 shall be set to zero; release interrupt is not supported.

Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.

Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 82 is obsolete.

Bit 12 of word 82 shall be set to one; the device supports the Write Buffer command.

Bit 13 of word 82 shall be set to one; the device supports the Read Buffer command.

Bit 14 of word 82 shall be set to one; the device supports the NOP command.

Bit 15 of word 82 is obsolete.

Bit 0 of word 83 shall be set to zero; the device does not support the Download Microcode command.

Bit 1 of word 83 shall be set to zero; the device does not support the Read DMA Queued and Write DMA Queued commands.

Bit 2 of word 83 shall be set to one; the device supports the CFA feature set.

If bit 3 of word 83 is set to one, the device supports the Advanced Power Management feature set.

Bit 4 of word 83 shall be set to zero; the device does not support the Removable Media Status feature set.

### Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by device prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.

If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command.

Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.

If bit 5 of word 85 is set to one, write cache is enabled.

If bit 6 of word 85 is set to one, look-ahead is enabled.

Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.

Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.

Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 85 is obsolete.

Bit 12 of word 85 shall be set to one; the device supports the Write Buffer command.

Bit 13 of word 85 shall be set to one; the device supports the Read Buffer command.

Bit 14 of word 85 shall be set to one; the device supports the NOP command.

Bit 15 of word 85 is obsolete.

Bit 0 of word 86 shall be set to zero; the device does not support the Download Microcode command.

Bit 1 of word 86 shall be set to zero; the device does not support the Read DMA Queued and Write DMA Queued commands.

If bit 2 of word 86 shall be set to one, the device supports the CFA feature set.

If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.

Bit 4 of word 86 shall be set to zero; the device does not support the Removable Media Status feature set.

### Word 88: Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported.

Bits 15-13: Reserved

Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected

Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected

Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected

Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected

Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected

Bits 7-5: Reserved

Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 shall be set to 1.

Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 shall be set to 1.

Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 shall be set to 1.

Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.

Bit 0: 1 = Ultra DMA mode 0 is supported

### Word 93: Hardware Configuration test results

During hardware reset execution, Device 0 shall clear bits 13-8 of this word to zero and shall set bits 7-0 of the word as indicated to show the result of the hardware reset execution. During hardware reset execution, Device 1 shall clear bits 7-0 of this word to zero and shall set bits 13-8 as indicated to show the result of the hardware reset execution.

Bit 13 shall be set or cleared by the selected device to indicate whether the device detected CBLID- above VIH or below VIL at any time during execution of each IDENTIFY DEVICE routine after receiving the command from the host but before returning data to the host. This test may be repeated as desired by the device during command execution (see Annex B). Word 89 specifies the time required for the Security Erase Unit command to complete.

This command shall be supported on devices that support security.

**Notice:** CBLID- is grounded in the 80-conductor cable assembly host connector for the purpose of indicating to the host that the cable assembly being used is an 80-conductor assembly not a 40-conductor assembly.

The contents of bits 12-0 of this word shall change only during the execution of a hardware reset.

Bit 15: Shall be cleared to zero.

Bit 14: Shall be set to one.

Bit 13: 1 = dvice detected CBLID- above ViH

0 = device detected CBLID- below ViL

Bit 12-8: Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:

Bit 12: Reserved.

Bit 11: 0 = Device 1 did not assert PDIAG-.

1 = Device 1 asserted PDIAG-.

Bit 10-9: These bits indicate how Device 1 determined the device number:

00 = Reserved.

01 = a jumper was used.

10 = the CSEL signal was used.

11 = some other method was used or the method is unknown.

Bit 8: Shall be set to one.

Bit 7-0: Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:

Bit 7: Reserved.

Bit 6: 0 = Device 0 does not respond when Device 1 is selected.

1 = Device 0 responds when Device 1 is selected.

Bit 5: 0 = Device 0 did not detect the assertion of DASP-.

1 = Device 0 detected the assertion of DASP-.

Bit 4: 0 = Device 0 did not detect the assertion of PDIAG-.

1 = Device 0 detected the assertion of PDIAG-.

Bit 3: 0 = Device 0 failed diagnostics.

1 = Device 0 passed diagnostics.

Bit 2-1: These bits indicate how Device 0 determined the device number:

00 = Reserved.

01 = a jumper was used.

10 = the CSEL signal was used.

11 = some other method was used or the method is unknown.

Bit 0: Shall be set to one.

### Word 160: Power Requirement Description

This word is required for devices that support power mode 1.

Bit 15: VLD

If set to 1, indicates that this word contains a valid power requirement description.

If set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV

This bit is reserved and shall be 0.

Bit 13: -XP

If set to 1, indicates that the device does not have Power Level 1 commands.

If set to 0, indicates that the device has Power Level 1 commands

Bit 12: -XE

If set to 1, indicates that Power Level 1 commands are disabled.

If set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current

This field contains the device's maximum current in mA.

**(7) Identify Device DMA – EEh**

Bit ->	7	6	5	4	3	2	1	0
Command	EEh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Identify Device DMA**

This command enables the host to receive parameter information from the device in DMA mode. The command transfers the same 256 words of device identification data as transferred by the IDENTIFY DEVICE command. It is an obsolete command after ATA-4.

**(8) Idle - 97h or E3h**

Bit ->	7	6	5	4	3	2	1	0
Command	97h or E3h							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)					X			

**Idle**

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

**(9) Idle Immediate - 95h or E1h**

Bit ->	7	6	5	4	3	2	1	0
Command	95h or E1h							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Idle Immediate**

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

**(10) Initialize Drive Parameters - 91h**

Bit ->	7	6	5	4	3	2	1	0
Command	91h							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)	Number of Sectors							
Feature (1)					X			

**Initialize Drive Parameters**

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Device/Drive/Head registers are used by this command.

**(11) Media Lock – DEh**

Bit ->	7	6	5	4	3	2	1	0
Command	DEh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Media Lock**

It is implemented for compatibility and is no function in this device.

**(12) Media Unlock – DFh**

Bit ->	7	6	5	4	3	2	1	0
Command	DFh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Media Unlock**

It is implemented for compatibility and is no function in this device.

**(13) NOP – 00h**

Bit ->	7	6	5	4	3	2	1	0
Command	00h							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**NOP**

This command always fails with an aborted command error.

#### (14) Read Buffer - E4h

Bit ->	7	6	5	4	3	2	1	0
Command	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

#### Read Buffer

The Read Buffer command enables the host to read the current contents of the device's sector buffer. This command has the same protocol as the Read Sector(s) command.

#### (15) Read DMA – C8h

Bit ->	7	6	5	4	3	2	1	0
Command	C8h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

#### Read DMA

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the device sets BSY, puts all or part of the sector of data in the buffer. The Device is then permitted, although not required, to set DRQ, clear BSY. The Device asserts DMAREQ while data is available to be transferred. The Device asserts DMAREQ while data is available to be transferred. The host then reads the (512 \* sector-count) bytes of data from the Device using DMA. While DMAREQ is asserted by the Device, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Read DMA command is received by the Device and 8 bit transfer mode has been enabled by the Set Features command, the Device shall return the Aborted error.

**(16) Read Long Sector - 22h or 23h**

Bit ->	7	6	5	4	3	2	1	0
Command	22h or 23h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

**Read Long Sector**

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the device does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

**(17) Read Multiple - C4h**

Bit ->	7	6	5	4	3	2	1	0
Command	C4h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

**Read Multiple**

**Notice:** This specification requires that devices support a multiple block count of 1 and permits larger values to be supported.

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command. Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for  $n$  sectors, where

$$n = (\text{sector count}) \bmod (\text{block count}).$$

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

#### (18) Read Native Max Address – F8h

Bit ->	7	6	5	4	3	2	1	0
Command	F8h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

#### Read Native Max Address

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition. The native maximum address is the maximum address that is valid when using the SET MAX ADDRESS command.

#### (19) Read Sector(s) - 20h or 21h

Bit ->	7	6	5	4	3	2	1	0
Command	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

#### Read Sector(s)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the device sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block

Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

#### (20) Read Verify Sector(s) - 40h or 41h

Bit ->	7	6	5	4	3	2	1	0
Command	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

#### Read Verify Sector(s)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the device sets BSY.

When the requested sectors have been verified, the device clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

#### (21) Recalibrate - 1Xh

Bit ->	7	6	5	4	3	2	1	0
Command	1Xh							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

#### Recalibrate

This command is effectively a NOP command to the device and is provided for compatibility purposes.

#### (22) Request Sense - 03h

Bit ->	7	6	5	4	3	2	1	0
Command	03h							
C/D/H (6)			X	Drive	x			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

#### Request Sense

This command requests extended error information for the previous command. Table 8 defines the valid extended

error codes for the device Series product. The extended error code is returned to the host in the Error Register.

**Table 7: Extended Error Codes**

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed
22h	Power Level 1 Disabled

**(23) Seek - 7Xh**

Bit ->	7	6	5	4	3	2	1	0
Command	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

**Seek**

This command is effectively a NOP command to the device although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

**(24) Set Features – EFh**

Bit ->	7	6	5	4	3	2	1	0
Command	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

**Set Features**

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the Compact Flash Storage Device shall return command aborted. Table 9: Feature Supported defines all features that are supported.

**Table 8: Feature Supported**

Feature	Operation
01h	Enable 8 bit data transfers.
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Count register.
05h	Enable Advanced Power Management.
09h	Enable Extended Power operations. <b>(Alert!)</b> <i>It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.</i>
0Ah	Enable Power Level 1 commands.
44h	Product specific ECC bytes apply on Read/Write Long commands.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8 bit data transfer.
82h	Disable Write Cache.
85h	Disable Advanced Power Management.
89h	Disable Extended Power operations. <b>(Alert!)</b> <i>It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.</i>
8Ah	Disable Power Level 1 commands.
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
AAh	Enable Read Look Ahead.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses. The host shall not enable this feature for DMA transfers.

Features 02h and 82h allow the host to enable or disable write cache in devices that implement write cache. When the subcommand disable write cache is issued, the device shall initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Devices which support DMA, one Multiword DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

**Table 9: Transfer mode values**

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

If a device supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode

parameter and a Sector Count register value of “00000000b”, it shall set its default PIO mode. If the value is “00000001b” and the device supports disabling of IORDY, then the device shall set its default PIO mode and disable IORDY. A device shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.

Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.

A device reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported.

A device reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported.

If an Ultra DMA mode is enabled any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device. Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Table 9: Advanced power management levels show these values.

**Table 10: Advanced power management levels**

Level	Sector Count Value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.

Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the device with extended power.

Features 55h and BBh are the default features for the device; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature code 9Ah enables the host to configure the device to best meet the host system’s power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the device should consume. For example, if the Sector Count register were set to 6, the device would be

configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the device responds to the host with the range of values supported by the device. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The device shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

#### (25) Set Max Address – F9h

Bit ->	7	6	5	4	3	2	1	0
Command	F9h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							Volatile
Feature (1)	X							

#### Set Max Address

This command is used to set a temporary or permanent maximum address. After successful command completion, all read and write access attempts to addresses greater than the specified maximum address shall be rejected with an IDNF error. IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

After a successful SET MAX ADDRESS command using a new maximum LBA the content of all IDENTIFY DEVICE words (61:60) shall be equal to the new Maximum LBA + 1.

The LBA address in the command registers is the maximum address for the setting. Bit 0 in the Sector Count represents Value volatile.

If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset.

If bit 0 is cleared to zero, the device shall revert to the most recent non-volatile maximum address value setting over power-up or hardware reset.

#### (26) Set Multiple Mode - C6h

Bit ->	7	6	5	4	3	2	1	0
Command	C6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

#### Set Multiple Mode

This command enables the device to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the device sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and

execution is enabled for all subsequent Read Multiple and Write Multiple commands.

If the block count is not supported, an Aborted Command error is posted and the Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

#### (27) Set Sleep Mode- 99h or E6h

Bit ->	7	6	5	4	3	2	1	0
Command	99h or E6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

#### Set Sleep Mode

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

#### (28) SMART- B0h

Individual SMART commands are identified by the value placed in the Feature register. The following table shows these Feature register values for this device.

**Table 11: SMART Feature register values**

Value	Command
D0h	SMART Read Data
D2h	SMART Enable/Disable Attribute Autosave
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
E0h	(Vendor Specific SMART function): SMART Read Remap Data
E1h	(Vendor Specific SMART function): SMART Read Wear Level Data
Others	Reserved

**Notice:** If reserved size below the Threshold, the status can be read from Cylinder register by SMART Return Status command (DAh).

**• Feature D9h: SMART Disable Operations**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D9h							

**SMART Disable Operations**

This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After command acceptance the device shall disable all SMART operations. SMART data shall no longer be monitored or saved by the device. The state of SMART, either enabled or disabled, shall be preserved by the device across power cycles.

After receipt of this command by the device, all other SMART commands including SMART DISABLE OPERATIONS commands, with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.

**• Feature D2h: SMART Enable/Disable Attribute Autosave**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	00h or F1h							
Feature (1)	D2h							

**SMART Enable/Disable Attribute Autosave**

This command enables and disables the optional attribute autosave feature of the device. This command may either allow the device, after some vendor specified event, to save the device updated attribute values to nonvolatile memory; or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature (either enabled or disabled) shall be preserved by the device across power cycles.

A value of zero written by the host into the device's Sector Count register before issuing this command shall cause this feature to be disabled. Disabling this feature does not preclude the device from saving SMART data to non-volatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F1h written by the host into the device's Sector Count register before issuing this command shall cause this feature to be enabled. Any other meaning of this value or any other non-zero value written by the host into this register before issuing this command may differ from device to device. The meaning of any nonzero value written to this register at this time shall be preserved by the device across power cycles.

If this command is not supported by the device, the device shall return command aborted upon receipt from the host.

During execution of the autosave routine the device shall not set BSY to one nor clear DRDY to zero. If the device

receives a command from the host while executing the autosave routine the device shall begin processing the command within two seconds.

• **Feature D8h: SMART Enable Operations**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D8h							

**SMART Enable Operations**

This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

• **Feature D0h: SMART Read Data**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D0h							

**SMART Read Data**

This command returns the Device SMART data structure to the host. Table showed below defines the 512 bytes that make up the Device SMART data structure.

**Table 12: Device SMART Data Structure**

Offset	Value	Description
0-1	0004h	SMAT Structure Revision code
2-361	V	Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (No off-line data collection) (Fixed)
363	00h	Self-test execution status byte (Self-test completed) (Fixed)
364-365	0000h	Total time in seconds to complete off-line data collection activity (Fixed)
366	00h	Reserved
367	00h	Off-line data collection capability (No Off-line data collection) (Fixed)
368-369	0003h	SMART capability
370	00h	Error logging capability (No error logging) (Fixed)
371	00h	Reserved
372	00h	Short self-test routine recommended polling time (in minutes) (Fixed)
373	00h	Extended self-test routine recommended polling time (in minutes) (Fixed)
374-385	00h	Reserved
386-387	00h	Reserved

Offset	Value	Description
388-395	V	Reserved, vendor specification area
396-510	00h	Reserved
511	V	Data structure checksum

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

\* 4 Byte value : [MSB] [2] [1] [LSB]

- (0-1) Revision code

This revision code area defines the firmware revision for the device.

- (2-361) Attribute entries 1 to 30 (12 bytes each)

There are five attributes that are defined for this device. These return their data in the attribute section of the SMART data, using a 12 byte data field. Rest of the area is reserved.

- **Spare Block Count Attribute:** This attribute gives information about the amount of available spare blocks.

Offset	Value	Description
0	196	Attribute ID – Reallocation Count
1-2	0003h	Flags – Pre-fail type, value is updated during normal operation
3	V	Attribute value. The value returned here is the minimum percentage of remaining spare blocks over all flash chips, i.e. min over all chips: (100 × current spare blocks / initial spare blocks)
4-5	V	Initial number of spare blocks of the flash chip that has been used for the attribute value calculation.
6-7	V	Current number of spare blocks of the flash chip that has been used for the attribute value calculation.
8-9	V	Sum of the initial number of spare blocks for all flash chips.
10-11	V	Sum of the current number of spare blocks for all flash chips.

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold, the SMART Return Status command will indicate a threshold exceeded condition.

- **Erase Count Attribute:** This attribute gives information about the amount of flash block erases that have been performed.

Offset	Value	Description
0	229	Attribute ID – Erase Count Usage (vendor specific)
1-2	0003h	Flags – Pre-fail type, value is updated during normal operation
3	V	Attribute value. The value returned here is an estimation of the remaining device life, in percent, based on the number of block erases compared to the target number of erase cycles per flash block.
4-11	V	Estimated total number of block erases

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold, the SMART Return Status command will indicate a threshold exceeded condition.

- **Total ECC Errors Attribute:** This attribute gives information about the total number of ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1-2	0002h	Flags – Advisory type, value is updated during normal operation

Offset	Value	Description
3	64h	Attribute value. This value is fixed at 100.
4-7	V	Total number of ECC errors (correctable and uncorrectable)
8-11	-	Reserved

- **Correctable ECC Errors Attribute:** This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC errors
1-2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4-7	V	Total number of correctable ECC errors.
8-11	-	Reserved

- Total Number of Reads Attribute: This attribute gives information about the total number of flash read commands. This can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	232	Attribute ID – Number of Reads (vendor specific)
1-2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4-11	V	Total number of flash read commands.

- **UDMA CRC Errors Attribute:** This attribute gives information about the total number of UDMA CRC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	199	Attribute ID – UDMA CRC error rate
1-2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4-7	V	Total number of UDMA CRC errors
8-11	-	Reserved

- (368-369) SMART capabilities

The following describes the definition for the SMART capabilities bits.

- Bit 0 - If this bit is set to one, the device saves SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode. If this bit is cleared to zero, the device does not save SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode.
- Bit 1 - This bit shall be set to one to indicate that the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.
- Bits (15:2) (Reserved).

- (372) Self-test routine recommended polling time

The self-test routine recommended polling time shall be equal to the number of minutes that is the minimum recommended time before which the host should first poll for test completion status. Actual test time could be several times this value. Polling before this time could extend the self-test execution time or abort the test depending on the state of bit 2 of the off-line data capability bits.

- (511) Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

● **Feature DAh: SMART Return Status**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	DAh							

**SMART Return Status**

This command causes the device to communicate the reliability status of the device to the host. If a threshold exceeded condition is not detected by the device, the device shall set the LBA Mid register to 4Fh and the LBA High register to C2h. If a threshold exceeded condition is detected by the device, the device shall set the LBA Mid register to F4h and the LBA High register to 2Ch.

● **Feature E0h: SMART Read Remap Data (Vendor specific)**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	01h							
Feature (1)	E0h							

**SMART Read Remap Data (Vendor specific)**

This command returns one sector of spare block information. The information is the initial number of blocks (directly after the pre-format) per flash chip available for bad block remap, and the current number of blocks per flash chip available for bad block remap. The layout of the returned sector is:

Offset	Description
0-31	Initial number of replacement blocks for chips 0..15, 2 bytes per entry
32-63	Current number of replacement blocks for chips 0..15, 2 bytes per entry
64-511	Reserved

**• Feature E1h: SMART Read Wear Level Data (Vendor specific)**

Bit ->	7	6	5	4	3	2	1	0
Command	B0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2h							
Cyl Low (4)	4Fh							
Sec Num (3)	X							
Sec Cnt (2)	04h							
Feature (1)	E1h							

**SMART Read Wear Level Data (Vendor specific)**

This command will return four sectors of information regarding the status of the wear leveling. The information returned is the distribution of the blocks into the 1024 possible wear level classes. For each of the wear level classes, the number of blocks that have this class is returned in the data sectors.

The layout of the returned sectors is, with n the sector number from 0 to 3:

Offset	Description
0-1	Number of flash blocks that have wear level class $256*n+0$
2-3	Number of flash blocks that have wear level class $256*n+1$
.....	.....
508-509	Number of flash blocks that have wear level class $256*n+254$
510-511	Number of flash blocks that have wear level class $256*n+255$

i.e. the first sector returns the information for wear level classes 0 to 255, the second sector returns the information for wear level classes 256 to 511, and so on.

A block moves from one wear level class into the next when it reaches the number of erases that is specified as the “Wear Level Threshold” in the preformat. A common threshold number is 4095, this means that blocks in wear level class 0 have seen 0 to 4095 erases, blocks in wear level class 1 have seen 4096 to 8191 erases, and so on. Using this information, statements about the wear of the device, and of the estimated remaining life can be made. The useful range of wear level classes is 0 to 1022, class 1023 has blocks that are not subject to wear leveling, like the Anchor block.

**(29) Standby - 96h or E2h**

Bit ->	7	6	5	4	3	2	1	0
Command	96h or E2h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

**Standby**

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

**(30) Standby Immediate - 94h or E0h**

Bit ->	7	6	5	4	3	2	1	0
Command	94h or E0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Standby Immediate**

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

**(31) Translate Sector - 87h**

Bit ->	7	6	5	4	3	2	1	0
Command	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)					X			
Feature (1)					X			

**Translate Sector**

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 12 represents the information in the buffer. Please note that this command is unique to the device.

**Table 13: Translate Sector Information**

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h – 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A) <sup>1</sup>
1Bh-1FFh	Reserved

**Notice:** 1) A value of 0 indicates Hot Count is not supported.

**(32) Write Buffer - E8h**

Bit ->	7	6	5	4	3	2	1	0
Command	E8h							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

**Write Buffer**

The Write Buffer command enables the host to overwrite contents of the device's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

**(33) Write DMA – CAh**

Bit ->	7	6	5	4	3	2	1	0
Command	CAh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

**Write DMA**

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the device sets BSY, puts all or part of the sector of data in the buffer. The Device is then permitted, although not required, to set DRQ, clear BSY. The Device asserts DMAREQ while data is available to be transferred. The host then writes the (512 \* sector-count) bytes of data to the Device using DMA. While DMAREQ is asserted by the Device, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Write DMA command is received by the Device and 8 bit transfer mode has been enabled by the Set Features command, the Device shall return the Aborted error.

**(34) Write Long Sector - 32h or 33h**

Bit ->	7	6	5	4	3	2	1	0
Command	32h or 33h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

**Write Long Sector**

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state device, the four bytes of ECC transferred by the host may be used by the device. The device may discard these four bytes and write the sector with valid ECC data. This comm device and has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

**(35) Write Multiple Command - C5h**

Bit ->	7	6	5	4	3	2	1	0
Command	C5h							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

**Write Multiple Command**

**Notice:** This specification requires that devices support a multiple block count of 1 and permits larger values to be supported.

This command is similar to the Write Sectors command. The device sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block that contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$$n = (\text{sector count}) \text{ modulo } (\text{block count}).$$

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation shall be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial

block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector numbers of the sector where the error occurred. The Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

### (36) Write Multiple without Erase – CDh

Bit ->	7	6	5	4	3	2	1	0
Command	CDh							
C/D/H (6)	X1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

#### Write Multiple without Erase

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

### (37) Write Sector(s) - 30h or 31h

Bit ->	7	6	5	4	3	2	1	0
Command	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

#### Write Sector(s)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the device sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred.

The host may then read the command block to determine what error has occurred, and on which sector.

### (38) Write Sector(s) without Erase - 38h

Bit ->	7	6	5	4	3	2	1	0
Command	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

#### Write Sector(s) without Erase

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase Sector(s) command, a normal write sector operation will occur.

### (39) Write Verify - 3Ch

Bit ->	7	6	5	4	3	2	1	0
Command	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

#### Write Verify

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

## 4. Installation

### 4.1 Installation

**For Installation of SATA DiskOnModule to your system, please follow up below steps;**

1. Make sure your computer is turned off before you open the case.
2. Plug the SATA DiskOnModule carefully into the Serial ATA slot on your computer or host adapter.
3. Plug the SATA DiskOnModule into Serial ATA Power Cable with 5V
4. Check cable connections and SATA DiskOnModule is firm enough.

### 4.2 Partition

**For DOS Operating System :**

- To partition your new SATA DiskOnModule for example use Microsoft DOS program:

1. Insert a bootable DOS diskette into your diskette drive and restart your computer.
2. Insert a DOS program diskette that contains the **FDISK.EXE** and **FORMAT.COM** programs into your diskette drive. Use the same DOS version that is on your bootable diskette. At the A: prompt, type **FDISK** and press **ENTER**.
3. Select "Create DOS partition or logical DOS drive" by pressing **1**. Then press **ENTER**.
4. Select "**Create primary DOS partition**" by pressing **1** again. Then press **ENTER**. Create your first drive partition. If you are creating a partition that will be used to boot your computer (drive C), make sure that the partition is marked active.
5. Create an extended partition and additional logical drives as necessary, until all the space on your new hard drive has been partitioned.
6. When the partitioning is complete, **FDISK** reboots your computer.

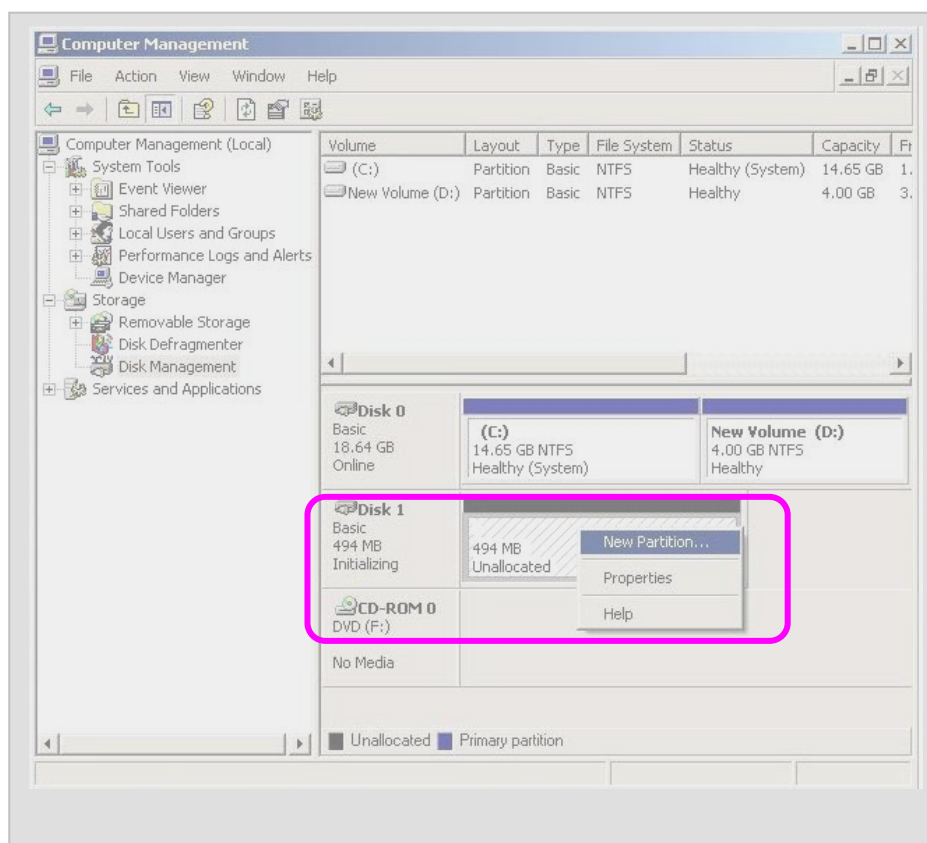
**Notice:** Make sure to use the correct drive letters so that you do not format a drive that already contains data.

7. At the A: prompt, type **format c:/s**, where c is the letter of your first new partition, Repeat the format process for all the new partitions you have created.
8. After you format your SATA DiskOnModule, it is ready to use.

**For Windows Operating System :**

- To partition your new SATA DiskOnModule, for example use Microsoft WindowsXP and WindowsXP embedded system :

1. In your windows system. You can Click the 『 Start 』 → 『 Control Panel 』 → 『 Administrative Tools 』 → 『 Computer Management 』 then select 『 Storage 』 → 『 Disk Manager 』 to setup the partition.



### 4.3 Format

#### For DOS Operating System :

- Before you format or partition your new SATA DiskOnModule, you must configure your computer's BIOS so that the computer can recognize your new SATA DiskOnModule.
  1. Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as DELETE, ESC, or F1, during startup. See your computer manual for details. Press the appropriate key to run the system setup program.
  2. If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option. (If you use Normal/CHS mode to partition your DOM, you can get the maximum formatted capacity.)  
This allows your computer to configure itself automatically for your new SATA DiskOnModule.  
If your BIOS does not provide automatic drive detection, select "User-defined" drive setting and enter the CHS values from the table.

#### BIOS Settings (see specification)

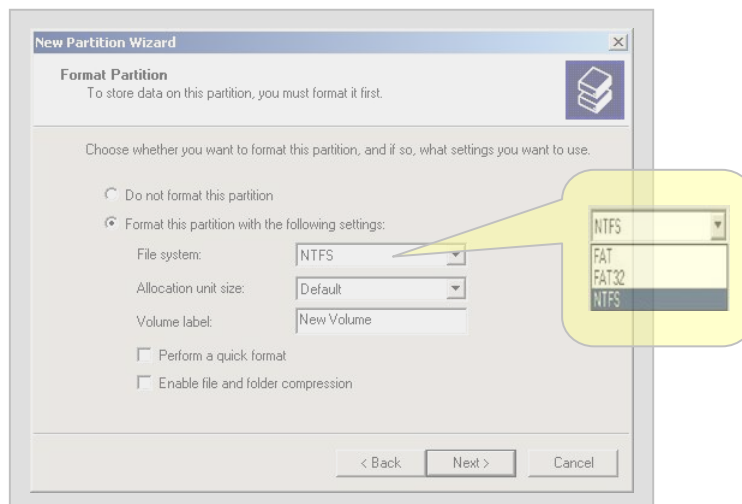
Capacity	Cylinders	Heads	Sectors	(unformatted)
----------	-----------	-------	---------	---------------

3. Save the settings and exit the System Setup program.  
(Your computer will be automatically rebooted.)

## For Windows Operating System :

- To partition your new DOM, for example use Microsoft WindowsXP and WindowsXP embedded system :

1. Click the 『 Start 』 → 『 Control Panel 』 → 『 Administrative Tools 』 → 『 Computer Management 』 then select 『 Storage 』 → 『 Disk Manager 』 to setup the file format.
2. Select “FAT or NTFS” format for user.



## 5. Troubleshooting

### 5.1 BIOS can not identify SATA DiskOnModule

- 5.1.1 Check Power Cable Status
- 5.1.2 Check Connector status
- 5.1.3 Check the Power Voltage (only 5V)

### 5.2 SATA DOM can not boot the system

- 5.2.1 Check BIOS setting
- 5.2.2 Reinstall your system

**Notice:** Please contact your closest CSS office for verifying your other troubles.

## 6. Ordering Information

HSH40(RB0/4) : 7+15P Horizontal SATA DiskOnModule.

**Table 14: 7+15Pin Horizontal SATA DiskOnModule Ordering Information**

P/N	Capacity	Note
HSH40- <sup>*1</sup> xxx <sup>G*2</sup> RB4 <sup>*3</sup> 0000	xGB	
HSH40-128MRB00000	128MB	Single Mode
HSH40-256MRB00000	256MB	Single Mode
HSH40-512MRB00000	512MB	Single Mode
HSH40-001GRB00000	1GB	Single Mode
HSH40-002GRB00000	2GB	Single Mode
HSH40-004GRB00000	4GB	Single Mode
HSH40-008GRB00000	8GB	Single Mode
HSH40-256MRB40000	256MB	Dual Mode
HSH40-512MRB40000	512MB	Dual Mode
HSH40-001GRB40000	1GB	Dual Mode
HSH40-002GRB40000	2GB	Dual Mode
HSH40-004GRB40000	4GB	Dual Mode
HSH40-008GRB40000	8GB	Dual mode
HSH40-016GRB40000	(Max) 16GB	Dual mode

\*1 : Operating temperature

-: normal temperature

W: wide temperature

\*2 : Capacity

128M: 128MB, 256M: 256MB, 512M: 512MB, 001G: 1GB, 002G: 2GB, 004G: 4GB, 008G: 8GB, 016G: 16GB

\*3 : Flash Density

0 : Single Mode (128MB~8GB)

4 : Dual Mode (256MB~16GB)

## 7. Contact Information

CoreSolid Storage Corporation, a TDK-PQI storage business company, specializes in the design and marketing of SSD, DOM, and Industry CF products.

For further information, please reach us at the following contact information:

For further information, please reach us at the following contact information:

### Global

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- Customer Service: [support@coresolid-storage.com](mailto:support@coresolid-storage.com)

### US specific

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- Sales: [sales@coresolid-storage.com](mailto:sales@coresolid-storage.com)
- Customer Service: [support.us@coresolid-storage.com](mailto:support.us@coresolid-storage.com)

### China specific

- Tel: +86-10-82701610
- Sales: [sales@coresolid-storage.com](mailto:sales@coresolid-storage.com)
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### Europe specific

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### Japan specific

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