

DiskOnModule

Standard II DJ Series



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1. Product Description

1.1 Product Overview

CoreSolid Storage designs DiskOnModule (DOM) in PQI brand name is the storage device based on NAND flash memory technology. This product complies with 40 PIN IDE (ATA) standard interface and is suitable for data storage media and code storage device for embedded system and boot disk. By using **DiskOnModule**, it is possible to operate good performance for the systems, which have IDE interface.

With small form factor, the applicable appliance can add or install IDE storage device on its Mother Board or Complete set.

● **Application Fields;**

- Industrial PC and Thin Client
- Game and Telecommunication Machine
- Ticketing, Examining, testing machine
- Army, Health and Production Equipment and Machine

1.2 Product Features

- Small form factor with IDE (ATA) Standard Interface connector
- Memory Capacities: 128MB ~ 4GB
- High performance and reliability
- Noiseless and stable installation to system
- Operating voltage 3.3V or 5.0V operation
- Standard IDE (ATA) Interface
- Master and Slave Switch
- Option model with Write Protection Switch
- Operating as Boot Disk
- Data Storage Device to 4GB
- Code Storage Device for Embedded Operating System

1.3 System Requirement

- The Host system which is connected to DiskOnModule should meet system requirements at minimum.

1.3.1 Power Requirement

- Voltage: DC +3.3V \pm 5% or DC +5.0V \pm 10%

1.3.2 Operating System

- Windows 2000/XP
- Linux
- DOS
- WinXP Embedded
- WinCE

1.3.3 Interface

- IDE (ATA) Standard Interface

2. Specification

2.1 Physical Specifications

2.1.1 Overlook

The overlook views of DiskOnModule are illustrated in Figure 1. Note the Write Protect Switch is an option model.

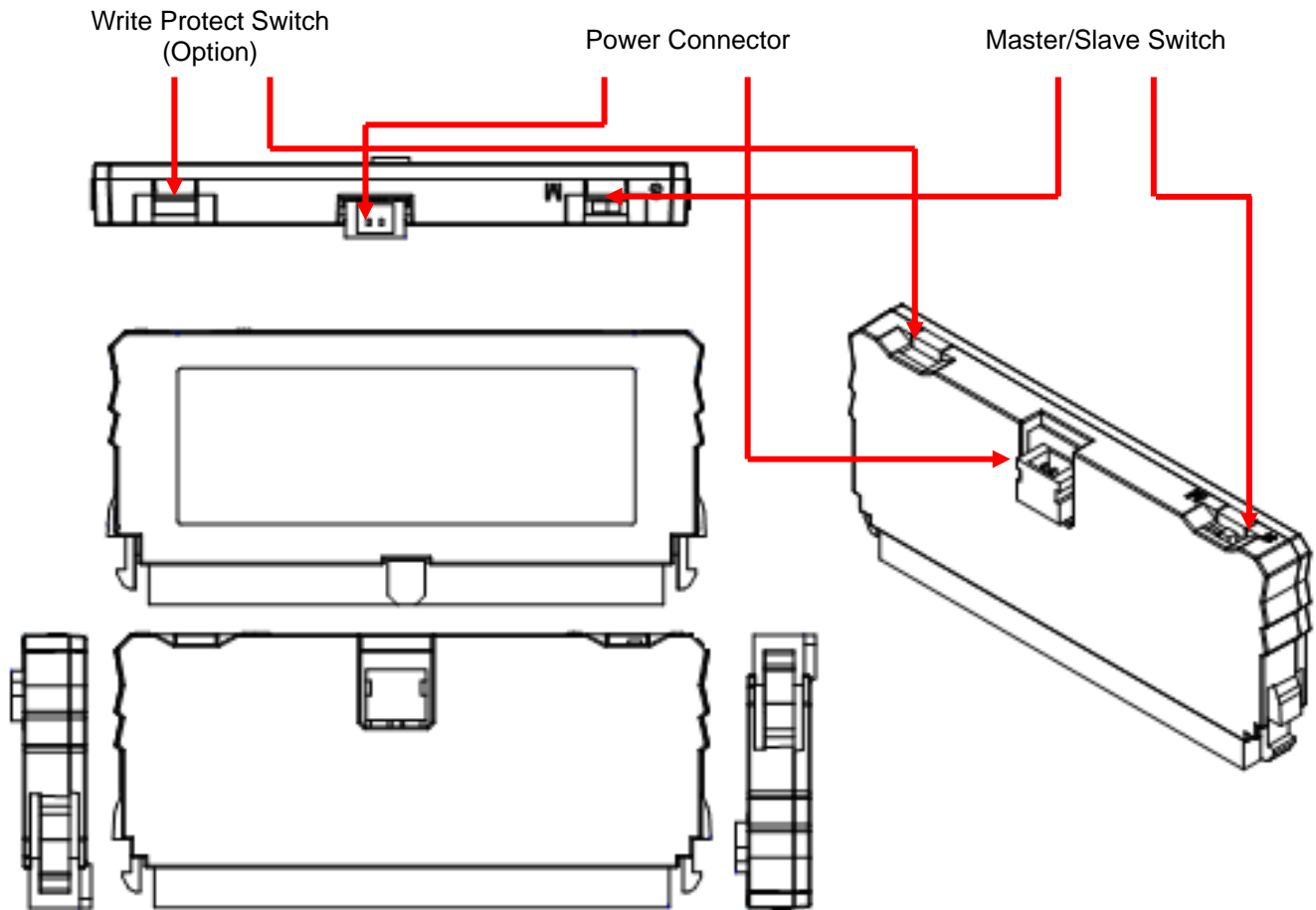


Figure 1: DiskOnModule Overlook Diagram

DiskOnModule

2.1.2 Dimension

The Dimensions of DiskOnModule are illustrated in Figure 2 and described in Table 1.

DJ0XXX46XX0 (40 PIN)

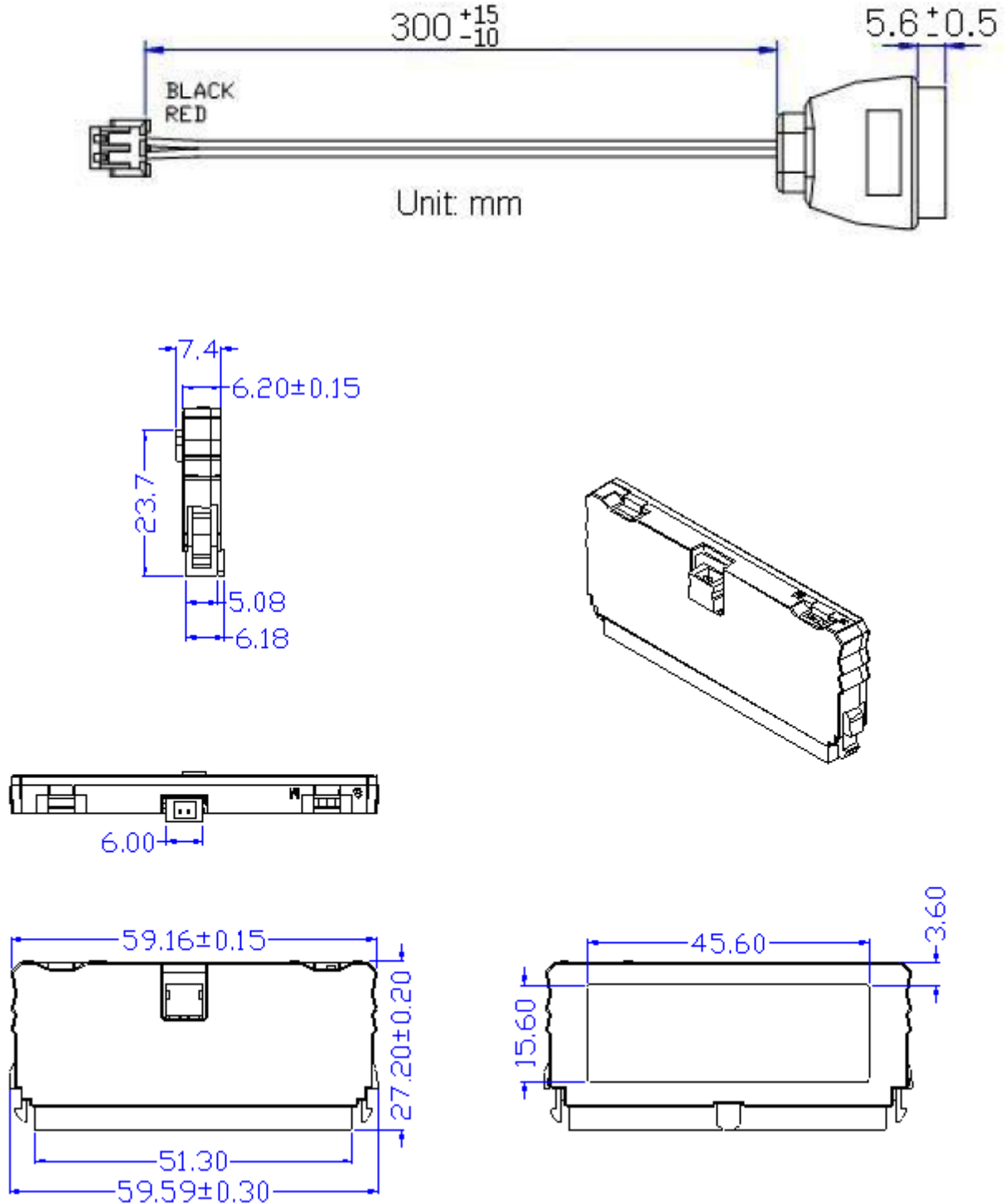


Figure 2: DOM Dimensions

Table 1: DiskOnModule Physical Dimension

Length	27.2 ± 0.2 mm
Width	59.2 ± 0.2 mm
Thickness	6.2 ± 0.2mm

2.1.3 Weight

- DiskOnModule Weight: < 12g
- Power Cable Weight: < 11g

2.2 Electronic Specifications

2.2.1 Product Definition

DiskOnModule is designed to operate and work as Data or Code Storage device by NAND Flash Memory and its Controller through IDE (ATA) Standard Interface to Host Systems.

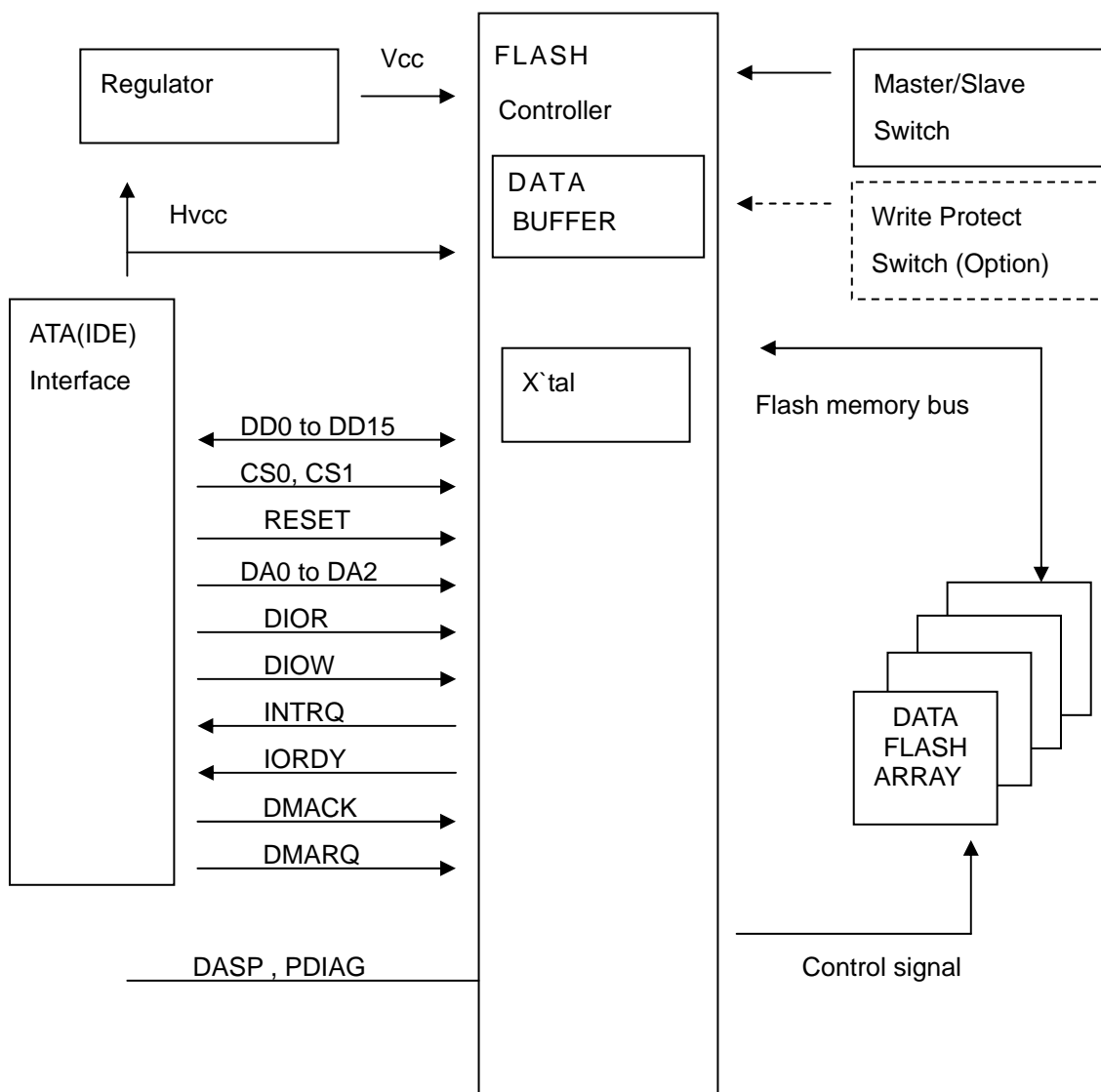


Figure 3: DiskOnModule Block Diagram

DiskOnModule

2.2.2 Operating Voltage

- Voltage DC +3.3V \pm 5% or DC +5.0V \pm 10%

2.2.3 Capacity and Block Size information

- Capacity: 128MB ~ 4GB
- Sector Size: 512B

2.2.4 Power Consumption

- DC Information

Test Item	3.3V	5.0V
Write Current	45mA	48mA
Read Current	43mA	45mA
Sleep Current	0.6mA	0.8mA

※ Testing Platform;

- Mother-Board: GA-K8U-939, CPU: K8 2.0G, System Memory: DDR 512MB,
 Operating System: DOS 6.22, Test Program: RWALL10 & DOMSV31

2.3 Performance Specifications

2.3.1 Modes

- PIO mode 4
- Multiword DMA 2
- Ultra DMA 2
- Setting to Ultra DMA 0 or 1 also available as following to Customer's request

2.3.2 Seek Time

- DiskOnModule has no seek time by being based on Flash Memory technology.

2.3.3 Mount Time

- The Mount Time for initializing and mounting DiskOnModule is different by depending on Operating System and testing Platform.

2.3.4 Data Transfer Time by Channel mode

Mode	Single		Dual Mode	
	Sequential Read	Sequential Write	Sequential Read	Sequential Write
Speed	Up to 10MB/s	Up to 5MB/s	Up to 20MB/s	Up to 10MB/s

※ Test Platform: GIGA 8I945GME Intel:945+ICH7 3.0GHz DDR:400

Testing Software: HD Bench 3.4 Testing OS: Windows XP

Notice

The value is various bases on the testing platform.

2.3.5 Data Retention

- 10years without requiring power support

2.3.6 Wear-leveling

- Dynamic Wear-Leveling for same level of Write/Erase Cycle

2.3.7 Bad Block Management

- The Bad Blocks of Flash Memory will be replaced into new ones by controller.

2.4 Environmental Specifications

2.4.1 Temperature

- Operating Temperature: 0°C to +70°C, Non Operating Temperature: -40°C to +85°C (Industrial type)
- Operating Temperature: -40°C to +85°C, Non Operating Temperature: -55°C to +95°C (Wide Temperature type)

2.4.2 Humidity

- Operating Humidity: 10% to 95%
- Non-Operating Humidity: 10% to 95% (with no condensation relative humidity)

2.4.3 Vibration

- Random Vibration (Operation) : Testing Specification

Frequency (Hz)	PSD (G ² /Hz)	Acceleration (Grms)	Dwell Time (Min)
10	0.01	6Grms	30min per axis (X · Y · Z)
100	0.08		
500	0.08		

- Sine Vibration (Non-Operation) : Testing Specification

Testing Specification		
Frequency (Hz)	Acceleration (G)	Dwell Time (min)
10~500 Hz	15 G	30min per axis (X · Y · Z)

2.4.4 Bare Drop Testing

- Testing Conditions: 75cm height
- Testing Orientation: (Free fell) Front/Rear/Right/Left/Top/Bottom side
- Testing Result: Pass

2.5 Reliability Specifications

2.5.1 ECC/EDC (Error Correction Code/Error Detection Code)

- Built-in Reed Solomon 4bytes/sector correction and 5bytes/sector detection.

2.5.2 Read and Write/Erase Cycle

- Read: No Limitation
- Write/Erase: 5,000,000 times
(Estimated on reference to Doc No.SM070001)

2.5.3 MTBF (Mean Time Between Failure)

- 2,000,000 hours
(Estimated on reference to Doc No.SM070002)

2.5.4 Power Cycle

- The Power Cycling is tested to 5000 loop. => "Pass"

2.6 Compliance Specifications

- CE
- FCC

※ Note: Please contact your closest CSS office for other certificate information.

3. Function

3.1 Switch Setting

3.1.1 Master/Slave Switch

- On case which the switch place “Master” side, then the DOM will be recognized as C: Drive in system and operate as main storage device.
- On case of placing in “Slave” side, the DOM will be recognized as slave disk and operate as slave storage device.

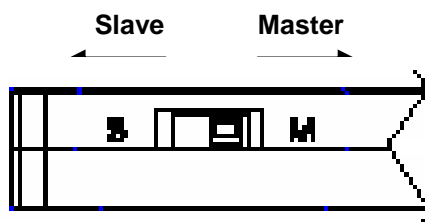


Figure 4: Master/Slave Function Switch

3.1.2 Write Protect Switch (Option model)

- On case which the switch place “Lock” side, then the data can not be written into DOM and can be read only.
- On case of placing in “Unlock” side, the data can be written and read together.

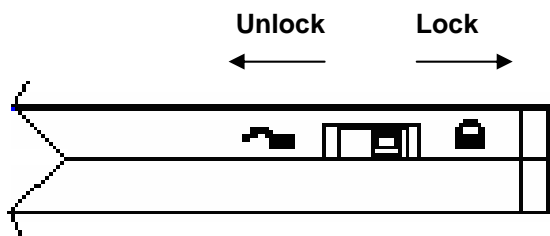


Figure 5: Write Protect Switch (Option Model)

3.2 Pin Signal Assignment

- The signals assigned for ATA applications are described in Table 2

Table 2: ATA connector pin definitions

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin) or Vcc
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground

※ Notes:

1. All pins are in a single row, with a 2.54 mm (0.100") pitch.
2. The comments on the mating sequence apply to the case of backplane blind mate connector only. In this case, the mating sequences are:
 - - the pre-charge power pints and the other ground pins.
 - - the signal pins and the rest of the power pins.

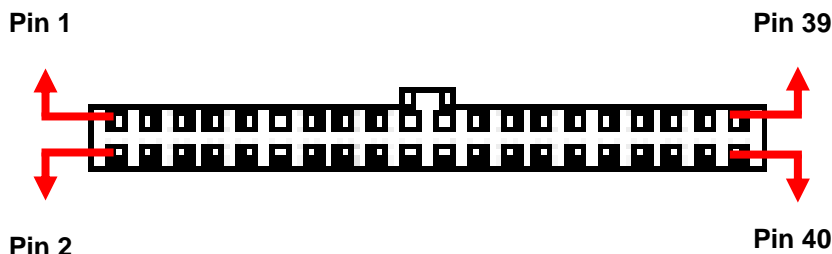


Figure 6: Signal Connector

3.3 Support ATA Commands

● ATA Command Set

- ATA Command Set summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 3: CF-ATA Command Set List

Command	Command code	Used parameter					
		FR	SC	SN	CY	DH	LBA
CFA ERASE SECTOR(S)	C0H	-	Y	Y	Y	Y	Y
CFA REQUEST EXTENDED ERROR CODE	03H	-	-	-	-	D	-
CFA TRANSLATE SECTOR	87H	-	-	Y	Y	Y	Y
CFA WRITE MULTIPLE WITHOUT ERASE	CDH	-	Y	Y	Y	Y	Y
CFA WRITE SECTOR(S) WITHOUT REASE	38H	-	Y	Y	Y	Y	Y
Check power mode	E5H or 98H	-	-	-	-	D	-
Execute drive diagnostic	90H	-	-	-	-	-	-
Flush cache	E7H						
Format track	50H	-	Y	Y	Y	Y	Y
Identify Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle immediate	E1h or 95h	-	-	-	-	D	-
Initialize drive parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read buffer	E4H	-	-	-	-	D	-
Read DMA	C8h,C9h	-	Y	Y	Y	Y	Y
Read long sector	22H or 23H	-	-	Y	Y	Y	Y
Read multiple	C4H	-	Y	Y	Y	Y	Y
Read sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read verify sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
Recalibrate	1Xh	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set features	EFH	Y	-	-	-	D	-
Set multiple mode	C6H	-	Y	-	-	D	-
Set sleep mode	E6h or 99h	-	-	-	-	D	-
Stand by	E2h or 96h	-	-	-	-	D	-
Stand by immediate	E0h or 94h	-	-	-	-	D	-

Write buffer	E8H	-	-	-	-	D	-
Write DMA	CAH,CBH	-	Y	Y	Y	Y	Y
Write long sector	32h or 33h	-	-	Y	Y	Y	Y
Write multiple	C5H	-	Y	Y	Y	Y	Y
Write sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write verify	3CH	-	Y	Y	Y	Y	Y
Wear level	F5H	-	-	-	-	D	-

Definitions:

FR = Features Register

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Registers

DH = Card/Drive/Head Register

LBA = Logical Block Address Mode Supported (see command descriptions for use).

Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Storage Card and head parameters are used; D - only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command descriptions for use).

(1) CFA ERASE SECTORS (C0h)

When this command is received, the flash memory corresponding to the specified sector addressed is erased units of physical blocks. If the address range for which erase is requested does not cover the whole page of a physical block, reading of this sector becomes unreliable after this command is executed so that the physical block will not be erased. To make this command function effectively, there is a need to take into account the descriptions of CFAWRITE MULTIPLE WITHOUT ERASE command. Note that it is impossible to recover the erased data using a utility tool after this command is executed because this command erases the data in the flash memory electrically.

If the last sector is exceeded while erasing data, after the data in the last sector is erased, the command is completed with an address overflow.

[Saving the Erased Range]

The address range specified with this command will be saved. When an address range succeeding a saved address range is newly specified with this command, the command is executed with both the saved address range and the newly specified address range considered to be the address range to be erased. Therefore, if a physical block which was not covered by the address range specified with the previous command and not erased is covered by the address range specified with the next command, this block will be erased.

If the newly specified address range succeeds or overlaps the saved address range, the address range covering the two address ranges is considered as a new address range to be saved.

If the new address range specified with this command does not succeed a saved address range, then when a write related command is issued, or when a reset operation (power-on reset, hardware reset, or each software reset) is performed, or when it goes into vendor mode, the saved address range will be cleared.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA			
Command	C0h							

Sector Count register: : The number of sectors to be erased (256 sectors in the case of 00h)

Sector Number register: : Starting sector address to be erased (CHS: Sector address/LBA: LBA [7:0])

Cylinder Low register: : Starting sector address to be erased (CHS: Lower cylinder address/LBA: LBA [15:8])

Cylinder High register: : Starting sector address to be erased (CHS: Upper cylinder address/LBA: LBA [23:16])

Device/Head register: : Starting sector address to be erased (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA[7:0]							
Cylinder Low	Cylinder Low or LBA[15:8]							
Cylinder High	Cylinder High or LBA[23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA[27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h

Sector Count register: : 00h

Sector Number register: : Last erased sector address (CHS: Sector address/LBA: LBA [7:0])

Cylinder Low register: : Last erased sector address (CHS: Lower cylinder address/LBA: LBA [15:8])

Cylinder High register: : Last erased sector address (CHS: Upper cylinder address/LBA: LBA [23:16])

Device/Head register: : Last erased sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(2) CFA REQUEST EXTENDED ERROR CODE (03h)

This command is used to obtain detailed information on an error from the preceding command and return the information described below. After this command is received, the error information on the preceding command is set into the Error register. If any reset (reset of power-on, hardware, or software reset) is done between the preceding command and this command, the values returned by this command are not valid.

Feature	Operation
00h	No error detected
01h	No fault detected during the self-diagnosis
03h	Writing or erasing failed
05h	Diagnostic failed
09h	Other errors
0Ch	Media format damaged
10h,14h	ID Not Found
11h	Uncorrectable ECC error
11h	A reading error detected and automatically corrected
1Fh	Command abortion due to a transfer error
20h	An invalid command issued
21h	Invalid address information (Invalid head No. or sector No.)
2Fh	Address overflowed (too large)
11h	11h Read recovery error
3Ah	3Ah No spare sectors
3Dh	3Dh Address conversion error

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	03h							

Device/Head register: : Drive No.

In the case of normal completion

Register	7	6	5	4	3	2	1	0
Features	Extended error code							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

Error register: : See the codes shown in the above table.

(3)CFA TRANSLATE SECTOR (87h)

This command is used to provide information on the erased state and the writing times of a specified sector to the host.

With regard to the information returned by this device, see the TRANSLATE SECTOR information described below.

The Erased Flag (byte 13h) is set to FFh when a physical block corresponding to a specified sector is in the erased state, and set to 00h in the non-erased state. However, it is fixed to 00h in this device. The Hot Count bytes (18h – 1Ah) are always set to 00 00 00h.

In the bytes from 00h to 06h, the sector address information specified by the task file register is stored. From 04h to 06h, 24-bit data of the LBA address information excluding the upper 4 bits is set.

TRANSLATE SECTOR Information Specifications

Address in Sector	Data
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MBS (04) – LBA LSB (06)
07h-06h	Reserved
11h	Erased Flag
14h,17h	Reserved
18h-1Ah	00 00 00h (fixed)
1Bh-1FFh	FFh Reserved

Reserved means 00h.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector Number Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	87h							

Sector Number register: : Specified sector address (CHS: Sector address/LBA: LBA [7:0])

Cylinder Low register: : Specified sector address (CHS: Lower cylinder address/LBA: LBA [15:8])

Cylinder High register: : Specified sector address (CHS: Upper cylinder address/LBA: LBA [23:16])

Device/Head register: : Specified sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	Sector Number Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))
 Sector Number register: : Specified sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Specified sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Specified sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Specified sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(4) CFAWRITE MULTIPLE WITHOUT ERASE (CDh)

This command is treated in the same way as the WRITE MULTIPLE command. However, this device can erase a physical block including the sector targeted by the write operation in the case that CFA ERASE SECTORS command is issued together with a sector length exceeding the physical block size. Thus, in all the commands related to the write operation, the writing speed can be improved.

When the last sector is exceeded during the write operation, the command is completed with an address overflow error after the write operation to the last sector is finished.

Supplemental Information

To maximize the performance increase of advance erasure, it is necessary to match the cluster size to the erased block size of the NAND flash memory that is mounted during logical formatting, and to set the starting sector of the user area to page 0 of the flash memory.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector Number Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	CDh							

Sector Count register: : The number of sectors to be written (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be written (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be written (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be written (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be written (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	Sector Number Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last written sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last written sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last written sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last written sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(5) CFA WRITE SECTORS WITHOUT ERASE (38h)

This command is treated in the same way as the WRITE SECTOR (S) command. With regard to the method of improving the write speed using advance erasure in this device, see CFAWRITE MULTIPLEWITHOUT ERASE command.

When the last sector is exceeded during the write operation, the command is completed with an address overflow error after the write operation to the last sector is finished.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	38h							

- Sector Count register: : The number of sectors to be written (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be written (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be written (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be written (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be written (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

- Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last written sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last written sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last written sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last written sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(6) CHCKE POWER MODE (98h or E5h)

This mode is used to return the present power mode. Whether the automatic power down is enabled or disabled in this device is returned. If the automatic power down mode is enabled, 00h is set to the Sector Count register. If the automatic power down mode is disabled, FFh is set to the Sector Count register. The execution of this command does not affect the operation mode of the power management function.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	98h or E5h							

- Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0	
Error	na								
Sector Count	result								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR	

Status register: : 50h (10h when DRDY is not set (1))

Sector Count register: : 00h (In the case that automatic power down is enabled)

: FFh (In the case that automatic power down is disabled)

(7) EXECUTE DEVICE DIAGNOSTIC (90h)

This command is used to check whether or not there is a fatal error in this device and return Diagnostic Codes as shown in the table below to the host. In the PC Card mode, the diagnosis results of this device only are returned, and slave devices are not supported. In the TrueIDE mode, only in the case that this device works as the master and there is a slave device, the diagnosis results of slave devices together with those of this device are returned. For information on how the master obtains the diagnosis results of slave devices, and on how it returns the diagnosis results when it works as a slave, see the ATA standard.

Diagnostic Code after Power On Reset or EXECUTE DEVICE DIAGNOSTIC command

Code	Description
01h	No error
06h	Fatal error found
07h	Fatal error during boot
8Xh	Slave error in the TrueIDE mode

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na							
Command	90h							

D4 (Device No.) of the Device/Head register is not evaluated. This command is executed for both the master and slaves.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	Diagnostic code							
Sector Count	01h							
Sector Number	01h							
Cylinder Low	00h							
Cylinder High	00h							
Device/Head	A0h							
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

Error register: : See the codes shown in the above table.

(8) FLUSH CACHE (E7h)

Although this command is usually used to write data in the cache to the flash, it is considered as a NOP process in this device.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	E7h							

Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

(9) FORMAT TRACK (50h)

This command is treated as NOP. The command protocol is the 1-sector PIO OUT protocol (command related to the write operation). This command is not supported by the ATA -4 and subsequent versions of the ATA standard. Also, the CFA standard does not recommend the use of this command.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	50h							

Sector Count register: : The number of sectors to be formatted (256 sectors in the case of 00h)

Sector Number register: : Sector address to be formatted (CHS: Sector address/LBA: LBA [7:0])

Cylinder Low register: : Sector address to be formatted (CHS: Lower cylinder address/LBA: LBA [15:8])

Cylinder High register: : Sector address to be formatted (CHS: Upper cylinder address/LBA: LBA [23:16])

Device/Head register: : Sector address to be formatted (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

Sector Count register: : 00h

Sector Number register: : Last formatted sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last formatted sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last formatted sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last formatted sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA fl

(10) IDENTIFY DEVICE (ECh)

This command is used to be used for the host to receive the drive parameter information. It returns 1-sector data to the host. With regard to the returned values of the drive parameter information, see the appendix (IDENTIFY DEVICE Information Specifications).

Input parameters

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	ECh							

Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

(11) IDLE (97h or E3h)

This command is meant to make the device go into the idle state of the ATA standard, but, in this device, it is only used to change the settings of the automatic power down sequence. When the Sector Count register is not 00h, the automatic power down sequence is executed, and immediately countdown is started. (Within the time equivalent to the numeric value of the Sector Count register multiplied by approx. 5ms, the device goes into the automatic power down sequence.) When the Sector Count register is 00h, the automatic power down sequence is prohibited until the register is reset. (For more information, see "Power Management Function.")

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Timer period value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	97h or E3h							

Device/Head register: : Drive No.

Sector Count register: : Constant of the automatic power down timer

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0	
Error	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR	

Status register: : 50h (10h when DRDY is not set (1))

(12) IDLE IMMEDIATE (95h or E1h)

This command is treated as NOP in this device.

Input parameters

Register	7	6	5	4	3	2	1	0	
Features	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Command	95h or E1h								

Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0	
Error	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR	

Status register: : 50h (10h when DRDY is not set (1))

(13) INITIALIZE DEVICE PARAMETERS (91h)

By issuing this command, the host is able to specify the number of sectors (8 bits) per track and the value (4 bits) calculated by the number of heads per cylinder – 1. This command does not check the validity of the number of sectors and the number of heads. If they are invalid values, an IDNF error is reported when an invalid access from other commands occurs. When the number of cylinders calculated by provided parameters exceeds FFFFh, FFFFh is returned to the 54th word of the parameter which is returned to IDENTIFY DEVICE command, and this value is also used for the address conversion from CHS to LBA.

Input parameters

Register	7	6	5	4	3	2	1	0	
Features	na								
Sector Count	logical sector number per track								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	Max Head				
Command	91h								

Sector Count register: : The number of sectors per track

Device/Head register: : Drive No., The number of heads –1

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0	
Error	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR	

Status register: : 50h (10h when DRDY is not set (1))

(14) NOP (00h)

This command is always terminated abnormally.

Input parameters

Register	7	6	5	4	3	2	1	0	
Features	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Command	00h								

Device/Head register: : Drive No.

(15) READ BUFFER (E4h)

This command enables the host to read data equivalent to 1 sector from the host buffer.

Input parameters

Register	7	6	5	4	3	2	1	0	
Features	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Command	E4h								

Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0	
Error	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR	

Status register: : 50h (10h when DRDY is not set (1))

(16) READ DMA (C8h or C9h)

This command is used to read data equivalent to the number of sectors specified in the Sector Count register starting from the sector number specified in the task file register, and to send it to the host in the DMA mode. It can read from 1 to 256 sectors. When 00h is set to the Sector Count register, data transfer equivalent to 256 sectors is processed. DRQ is set in the same way as READ SECTOR (S) command, and an interruption occurs only when the command is completed. When the command is completed, the last read sector is set in the task file register.

If an error occurs while the command is being executed, the ERR bit is set to the Status register after all the specified sectors are sent. Data after an error occurs are not always valid.

Since this device has the host buffer, the content of the task file register is not necessarily an address on which the error occurred in the case of a read error.

Even if the 8-bit transfer is enabled by SET FEATURES command, this command is operated in 16 bits.

In the case that the read recovery function is enabled, the specifications of this device are as follows.

When a correctable error is detected while reading data from the flash memory, this device backs up the page data, including the data corrected inside the device, of the relevant block to a new block, of which data has been erased, and conduct a diagnosis for the block of which error was reported. At this point, the device continues the read operation in response to Read command from the host, and therefore it seems that the device works without an error when seen from the host. (Meanwhile, during recovery, the BSY output period lengthens because the transfer between the host and this device is stopped.)

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	C8h or C9h							

Sector Count register: : The number of sectors to be read (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be read (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be read (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be read (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be read (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last read sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last read sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last read sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last read sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(17) READ LONG SECTOR (22h or 23h)

Following the transfer of the user data in the requested sector, Only 1 sector of ECC information with 4-byte configuration is read as FFFFFFFFh. Regardless of the setting of Long command of SET FEATURES command, the number of ECC information additional bytes is 4 bytes in this command.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	22h or 23h							

Sector Number register: : Sector address to be read (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Sector address to be read (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Sector address to be read (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Sector address to be read (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Read sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Read sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Read sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Read sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(18) READ MULTIPLE (C4h)

This command is the same as READ SECTOR (S) command except that an interruption occurs not for each sector transfer but for each block transfer that consists of the number of sectors defined by SET MULTIPLE command. When the nLEN bit (bit 0 of the Device Control register) is set (1), an interruption does not occur. For the information on the number of block counts (the number of sectors that make up a block), see SET MULTIPLE command. To execute this command, Multiple command needs to be permitted by SET MULTIPLE command in advance.

When the last sector is exceeded during the reading operation, this command is terminated with an address overflow error after the data in the last sector is transferred to the host.

In the case that the read recovery function is enabled, the specifications of this device are as follows.

When a correctable error is detected while reading data from the flash memory, this device backs up the page data, including the data corrected inside the device, of the relevant block to a new block, of which data has been erased, and conduct a diagnosis for the block of which error was reported. At this point, the device continues the read operation in response to Read command from the host, and therefore it seems that the device works without an error when seen from the host. (Meanwhile, during recovery, the BSY output period lengthens because the transfer between the host and this device is stopped.)

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	C4h							

Sector Count register: : The number of sectors to be read (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be read (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be read (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be read (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be read (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(19) READ SECTOR(S) (20h or 21h)

This command is used to read data equivalent to the number of sectors specified in the Sector Count register starting from the sector number specified in the task file register. It can read from 1 to 256 sectors. When 00h is set to the Sector Count register, data transfer equivalent to 256 sectors is processed. Regardless of presence or absence of an error state, DRQ is always set (1) before data transfer. When the command is completed, the last read sector is set in the task file register. If an uncorrectable error occurs, the reading operation is terminated at the sector where the error occurs, and that sector address is set in the task file register. Even if an uncorrectable error occurs, read data is stored in the host buffer, and the DRQ bit is set (1).

When the last sector is exceeded during the reading operation, this command is terminated with an address overflow error after the data in the last sector is transferred to the host.

In the case that the read recovery function is enabled, the specifications of this device are as follows.

When a correctable error is detected while reading data from the flash memory, this device backs up the page data, including the data corrected inside the device, of the relevant block to a new block, of which data has been erased, and conduct a diagnosis for the block of which error was reported. At this point, the device continues the read operation in response to Read command from the host, and therefore it seems that the device works without an error when seen from the host. (Meanwhile, during recovery, the BSY output period lengthens because the transfer between the host and this device is stopped.)

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	20h or 21h							

Sector Count register: : The number of sectors to be read (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be read (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be read (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be read (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be read (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last read sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last read sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last read sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last read sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA fla

(20) READ VERIFY SECTOR(S) (40h or 41h)

This command is used to conduct ECC verification against the data equivalent to the number of sectors specified by the Sector Count register starting from the sector number specified by the task file register. When this command is completed, the last verified sector address is set to the task file register. If a read error occurs, verification is ended at the sector in which the error occurs, and the address of that sector is set to the task file register, and the number of sectors which have not verified yet is set to the Sector Count register.

When the last sector is exceeded during the reading operation, the command is terminated with an address overflow error if there is no error in the last sector.

In the case that the read recovery function is enabled, the specifications of this device are as follows. These are set separately from READ SECTOR (S) command.

When a correctable error is detected while reading data from the flash memory, this device backs up the page data,

including the data corrected inside the device, of the relevant block to a new block, of which data has been erased, and conduct a diagnosis for the block of which error was reported. At this point, the device continues the verification operation in response to Verify command from the host, and therefore it seems that the device works without an error when seeing from the host.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	40h or 41h							

Sector Count register: : The number of sectors to be verified (256 sectors in the case of 00h)
 Sector Number register: : Starting sector address to be verified (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be verified (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be verified (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be verified (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last verified sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last verified sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last verified sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last verified sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(21) RECALIBRATE (1Xh)

Although this command is usually used to move the head arm of a hard disk drive device to the cylinder 00h, there is no effect on operations in this device. After this command is completed, the register values are initialized.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na	LBA	na	DRV	na			
Command	1Xh							

Device/Head register: : Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	CHS:01h/LBA:00h							
Cylinder Low	00h							
Cylinder High	00h							
Device/Head	na			DRV	11h			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

CHS mode

Sector Number register: : 01h

Cylinder Low register: : 00h

Cylinder High register: : 00h

Head register: : 11h

LBA mode

Sector Number register: : 00h

Cylinder Low register: : 00h

Cylinder High register: : 00h

Head register: : 11h

(22) SEEK (7Xh)

Although this command is usually used to seek the track specified by the task file register, it is treated as NOP in this device.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	7Xh							

Sector Number register: : Sector address to be sought (CHS: Sector address/LBA: LBA [7:0])

Cylinder Low register: : Sector address to be sought (CHS: Lower cylinder address/LBA: LBA [15:8])

Cylinder High register: : Sector address to be sought (CHS: Upper cylinder address/LBA: LBA [23:16])

Device/Head register: : Sector address to be sought (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

Sector Number register: : Sought sector address (CHS: Sector address/LBA: LBA [7:0])

Cylinder Low register: : Sought sector address (CHS: Lower cylinder address/LBA: LBA [15:8])

Cylinder High register: : Sought sector address (CHS: Upper cylinder address/LBA: LBA [23:16])

Device/Head register: : Sought sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(23) SET FEATURES (EFh)

This command is used to change some of the operational settings of this device.

With regard to Disable/Enable Power Level 1 commands, an error is returned because they are not supported.

Feature	Support	Operation
01h	Support	Enable 8bit Data Transfer
02h	NOP	Enable write cache
03h	****	Set transfer mode based on value in Sector Count register. See the table below (Transfer Mode)
09h	No	Enable power Level 1 commands
55h	NOP	Disable Read Lock Ahead
66h	Support	Disable Power on Reset establishment of defaults at Soft Reset
69h	NOP	NOP – Accepted for backward compatibility
81h	Support	Disable 8bit Data Transfer
82h	NOP	Disable write cache
89h	No	Disable Power Level 1 commands
96h	NOP	NOP – Accepted for backward compatibility
97h	NOP	Accepted for backward compatibility
9Ah	NOP	NOP – Set the host current source capability
BBh	NOP	4bytes of data apply on READ/WRITE LONG commands
CCh	Support	Enable Power on Reset establishment of defaults at Soft Reset

* The 8-bit transfer is not permitted when the power is turned on or after the hardware and/or the PCMCIA software is reset.

Transfer Mode

Subcommand	specific Operation
00h, 01h	PIO default setting
08h	PIO mode 0 setting
09h	PIO mode 1 setting
0Ah	PIO mode 2 setting
0Bh	PIO mode 3 setting
0Ch	PIO mode 4 setting
20h	Multiword DMA mode 0 setting
21h	Multiword DMA mode 1 setting
22h	Multiword DMA mode 2 setting
40h	Ultra DMA mode 0 setting
41h	Ultra DMA mode 1 setting
42h	Ultra DMA mode 2 setting
Others	Not supported parameter error

Note)

If you specify a mode that is not supported, it results in a non-supported parameter error.

For information on the transfer mode setting, see IDENTIFY DEVICE commands related specifications

Input parameters

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Subcommand specific							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	EFh							

Device/Head register:

Drive No.

Features register :

Function change parameter (See the codes in the table above)

Sector Count register:

PIO mode value (When the Features register = 03h)

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0	
Error	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR	

Sector register: : 50h (10h when DRDY is not set (1))

(24) SET MULTIPLE MODE (C6h)

This command is used to permit or prohibit Multiple commands (READ MULTIPLE, WRITE MULTIPLE, and CFAWRITE MULTIPLE WITHOUT ERASE commands) by setting the number of block counts (i.e., the number of sectors that compose a block) for Multiple commands. When the Sector Count register is set to 01h, Multiple commands to be issued subsequently are permitted. When the Sector Count register is set to 00h, they are prohibited. If the register is set to other values, the Status register is set (1) to D0 (ABRT), and Multiple commands to be issued after that are prohibited. In this device, specification of only 1 sector for one block is supported.

Multiple commands are prohibited when the power is turned on or the hardware is reset.

When this command is executed, the setting values are reflected in the lower byte of the word 59 in the IDENTIFY DEVICE information. (If Multiple commands are prohibited, 00h is set.)

Input parameters

Register	7	6	5	4	3	2	1	0	
Features	na								
Sector Count	Sector Number per block								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Command	C6h								

Device/Head register: : Drive No.

Sector Count register: : Number of sectors per block

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0	
Error	na								
Sector Count	na								
Sector Number	na								
Cylinder Low	na								
Cylinder High	na								
Device/Head	na			DRV	na				
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR	

Status register: : 50h (10h when DRDY is not set (1))

(25) SLEEP (99h or E6h)

This mode is used to make the device go into the sleep mode regardless of the present power down mode. With this command, the device clears the BSY (to 0), causes an interruption if the nIEN bit (bit 0 of the Device Control register) is cleared (0), and then goes into the sleep mode. It returns from the sleep mode next time a command is issued from the host or the mode is reset.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	99h or E6h							

Device/Head register: : Drive No

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

(26) STANDBY (96h or E2h)

When this device receives this command, it goes into the sleep mode after approx. 5ms regardless of the value of the Sector Count register. This does not affect the power down mode value and timer count value.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	96h or E2h							

Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

(27) STANDBY IMMEDIATE (94h or E0h)

When this device receives this command, it goes into the sleep mode after approx. 5ms. This command performs the same operation as STANDBY command.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	94h or E0h							

Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

(28) WRITE BUFFER (E8h)

This command is used to rewrite the data in the host buffer into the pattern that can be transferred from the host. When the device receives this command, it resets the internal host buffer, and then writes the transferred data in the host buffer.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	E8h							

Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h (10h when DRDY is not set (1))

(29) WRITE DMA (CAh or CBh)

This command is used to write the data which was transferred from the host in the DMA mode equivalent to the number of sectors specified in the Sector Count register starting from the sector number specified in the task file register. When the Sector Count register is set to 0, it is processed as data transfer equivalent to 256 sectors. DRQ is set in the same way as WRITE SECTOR (S) command, and an interruption occurs only when the command is completed. When the command is completed, the last written sector is set in the task file register.

If an error occurs while the command is being executed, the ERR bit is set to the Status register after all the specified sectors are sent. Data after an error occurs are not written.

Since this device has the host buffer, the content of the task file register is not necessarily an address on which the error occurred in the case of a write error.

Even if the 8-bit transfer is enabled by SET FEATURES command, this command is operated in 16 bits.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	CAh or CBh							

Sector Count register: : The number of sectors to be written (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be written (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be written (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be written (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be written (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last written sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last written sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last written sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last written sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(30) WRITE LONG SECTOR (32h or 33h)

This command is used to receive 4-byte ECC information from the host after 512-byte sector data and write the sector data only. This command transfers only 1 sector (512 bytes + 4 bytes).

Regardless of the settings related to Long command of SET FEATURES command, ECC information handled by this command is 4 bytes.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	32h or 33h							

Sector Count register: : na
 Sector Number register: : Sector address to be written (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Sector address to be written (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Sector address to be written (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Sector address to be written (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Written sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Written sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Written sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Written sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(31) WRITE MULTIPLE (C5h)

This command is the same as WRITE SECTOR (S) command except that an interruption occurs not for each sector transfer but for each block transfer that consists of the number of sectors defined by SET MULTIPLE command. When the nIEN bit (bit 0 of the Device Control register) is set (1), an interruption does not occur. For the information on the number of block counts (the number of sectors that make up a block), see SET MULTIPLE command. To execute this command, Multiple command needs to be permitted by SET MULTIPLE command in advance.

When the last sector is exceeded during the write operation, the command is completed with an address overflow error after the write operation to the last sector is finished.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	C5h							

Sector Count register: : The number of sectors to be written (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be written (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be written (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be written (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be written (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last written sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last written sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last written sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last written sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(32) WRITE SECTOR(S) (30h or 31h)

This command is used to write data equivalent to the number of sectors specified in the Sector Count register starting from the sector number specified in the task file register. When the Sector Count register is set to 0, it is processed as data transfer equivalent to 256 sectors. When the command is completed, the last written sector is set in the task file register. Since this device has the host buffer, the content of the task file register is not necessarily an address on which the error occurred in the case of a write error.

When the last sector is exceeded during the write operation, the command is completed with an address overflow error after the write operation to the last sector is finished.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	30h or 31h							

Sector Count register: : The number of sectors to be written (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be written (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be written (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be written (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be written (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last written sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last written sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last written sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last written sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

(33) WRITE VERIFY (3Ch)

This command is used to write data to a sector and then read that sector to verify if there is a read error. If an error occurs, the command is suspended. Even if a correctable error occurs, no correction is made to the flash memory. When the last sector is exceeded during the write operation, the command is completed with an address overflow error after the write operation to the last sector is finished.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Command	3Ch							

Sector Count register: : The number of sectors to be written (256 sectors are transferred in the case of 00h)
 Sector Number register: : Starting sector address to be written (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Starting sector address to be written (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Starting sector address to be written (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Starting sector address to be written (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	Sector Number or LBA [7:0]							
Cylinder Low	Cylinder Low or LBA [15:8]							
Cylinder High	Cylinder High or LBA [23:16]							
Device/Head	na	LBA	na	DRV	Head or LBA [27:24]			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register: : 50h
 Sector Count register: : 00h
 Sector Number register: : Last written sector address (CHS: Sector address/LBA: LBA [7:0])
 Cylinder Low register: : Last written sector address (CHS: Lower cylinder address/LBA: LBA [15:8])
 Cylinder High register: : Last written sector address (CHS: Upper cylinder address/LBA: LBA [23:16])
 Device/Head register: : Last written sector address (CHS: Head address/LBA: LBA [27:24]), Drive No., LBA flag

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WEAR LEVEL (F5h)

This command is treated as NOP.

Input parameters

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Command	F5							

Device/Head register: : Drive No.

Output parameters in the case of normal completion

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	00h							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	na			DRV	na			
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	na	ERR

Status register:

50h (10h when DRDY is not set (1))

Sector Count register: : 00h

3.4 Firmware Upgrade

- The Firmware of DiskOnModule can not be upgraded by customers, so please contact your nearest CSS Office.

3.5 Standard-II Capacity and Cylinder, Head, Sector

The table show various capacities available for Standard-II series, if your platform does not support auto-detection function or Standard-II series is not identified, we advice can following below Cylinders, Heads, Sectors number to setting your platform.

Unformatted Disk Capacity	No. of Cylinders	No. of Heads	No. of Sectors	Disk Total Sector
128MB	480	16	32	245760
256MB	960	16	32	491520
512MB	975	16	63	982800
1GB	1950	16	63	1965600
2GB	3900	16	63	3931200
4GB	7801	16	63	7863408

4. Operation Specification

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	VCC	-0.3 ~ +5.6	V
Input voltage	Vin	-0.3 ~ +5.6	V

(Referenced to GND)

Electric characteristics

Vcc=3.14V~5.5V

Item	Symbol	Value			Unit	Measuring conditions
		Min.	Standard	Max.		
Input voltage (TTL level)	V _{IH}	2.0	-	*1	V	
	V _{IL}	-	-	0.7	V	
Output voltage	V _{OH}	2.2	-	*2	V	I _{OH} =-2mA~ -24mA
	V _{OL}	-	-	0.4	V	I _{OL} =2mA~ 24mA

4.2 Series termination required for Ultra DMA operation

Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes, Table 4 describes typical values for series termination at the host and the device.

Table 4: Typical Series Termination for Ultra DMA

Signal	Host Termination	Device Termination
-IORD (-HDMARDY, HSTROBE)	22 ohm	82 ohm
-IOWR (STOP)	22 ohm	82 ohm
-CS0, -CS1	33 ohm	82 ohm
A00, A01, A02	33 ohm	82 ohm
-DMACK	22 ohm	82 ohm
D15 through D00	33 ohm	33 ohm
DMARQ	82 ohm	22 ohm
INTRQ	82 ohm	22 ohm
IORDY (-DDMARDY, DSTROBE)	82 ohm	22 ohm
-RESET	33 ohm	82 ohm

Note – Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. Shows signals also requiring a pull-up or pull down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.

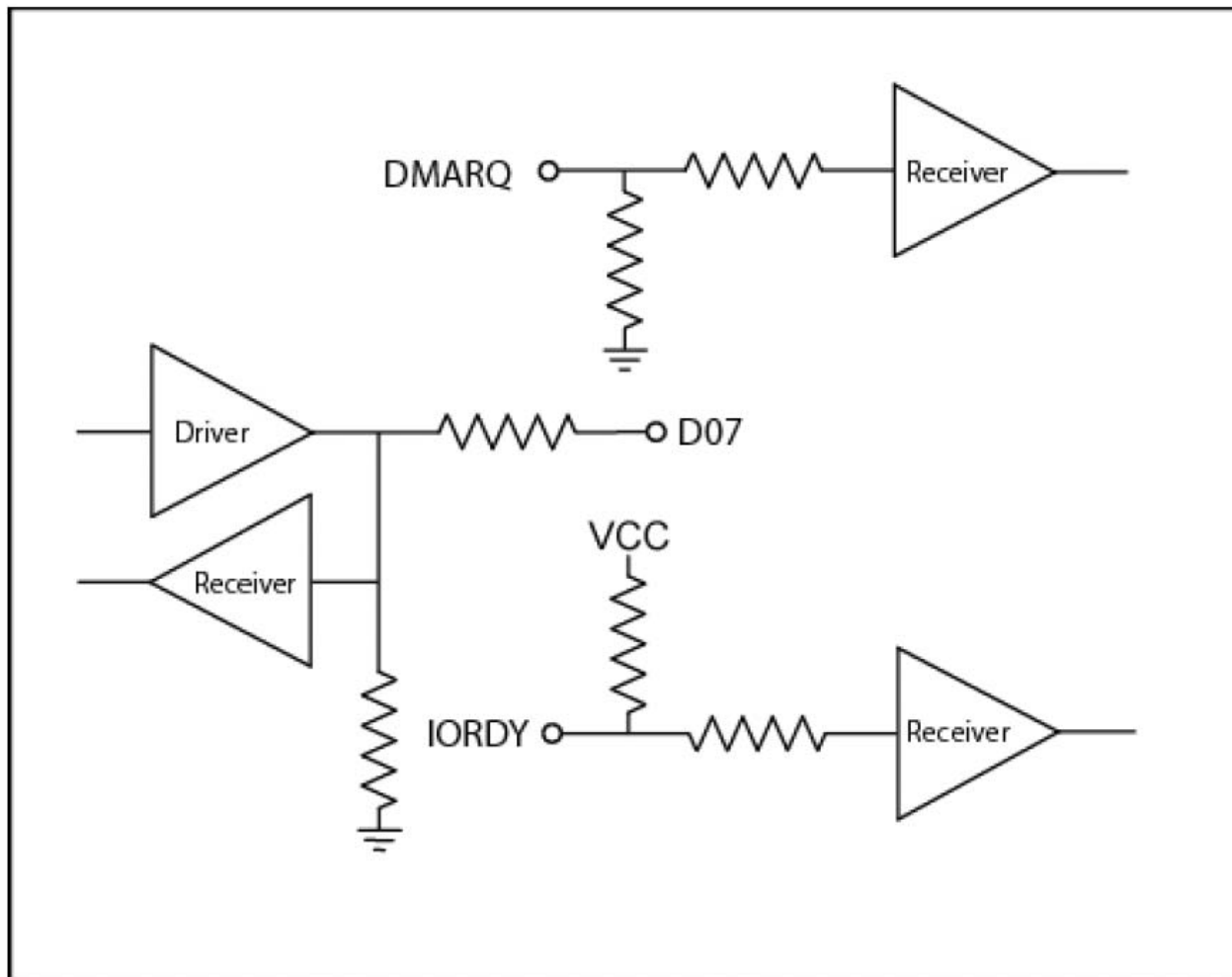


Figure 7: Ultra DMA termination with Pull-up or Pull down Example

4.3 True IDE PIO Mode Read/Write Timing Specification

The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD , the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 5: True IDE PIO Mode Read/Write Timing

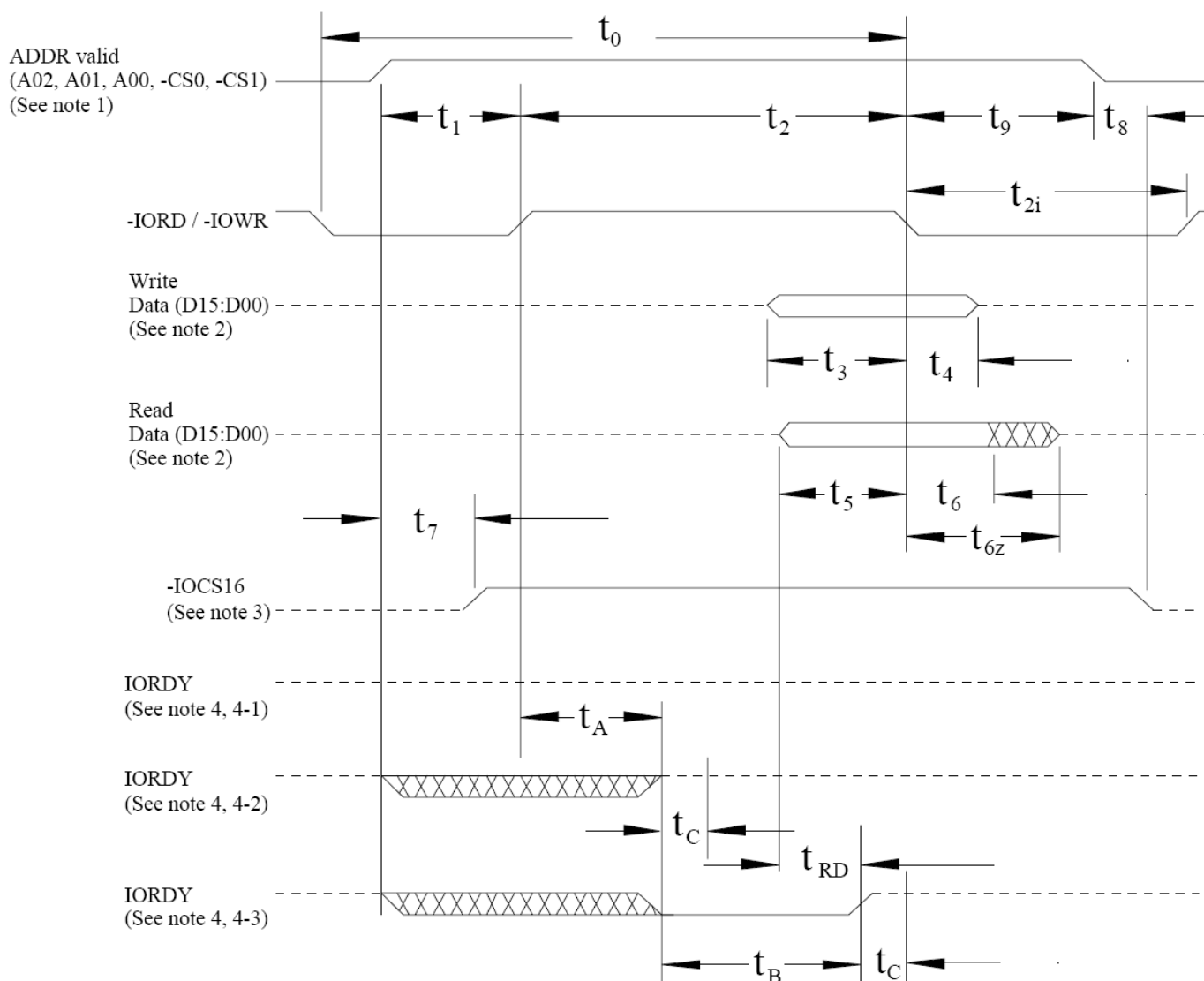
	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
t0	Cycle Time (min)	600	383	240	180	120	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	
t2	-IORD/-IOWR (min)	165	125	100	80	70	1
t2	-IORD/-IOWR (min) Register (8bit)	290	290	290	80	70	1
t2i	-IORD/-IOWR recovery time(min)	-	-	-	70	25	1
t3	-IOWR data setup (min)	60	45	30	30	20	
t4	-IOWR data hold (min)	30	20	15	10	10	
t5	-IORD data setup(min)	50	35	20	20	20	
t6	-IORD data hold (min)	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	4
t8	Address valid to -IOCS16	60	45	30	n/a	n/a	4

	released (max)						
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
tC	IORDY assertion to release(max)	5	5	5	5	5	

Note:

All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

- 1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time, The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data.
- 2) t7 and t8 apply only to modes0, 1 and 2. For other modes, this signal is not valid.
- 3) IORDY is not supported in this mode.



Notes:

- (1) Device address consists of -CS0, -CS1, and A[02::00]
- (2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
- (3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
- (4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
 - (4-1) Device never negates IORDY: No wait is generated.
 - (4-2) Device starts to drive IORDY low before t_A , but causes IORDY to be asserted before t_A : No wait generated.
 - (4-3) Device drives IORDY low before t_A : wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for t_{RD} before causing IORDY to be asserted.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Figure 8: True IDE PIO Mode Timing Diagram

4.4 True IDE Multiword DMA Mode Read/Write Timing Specification

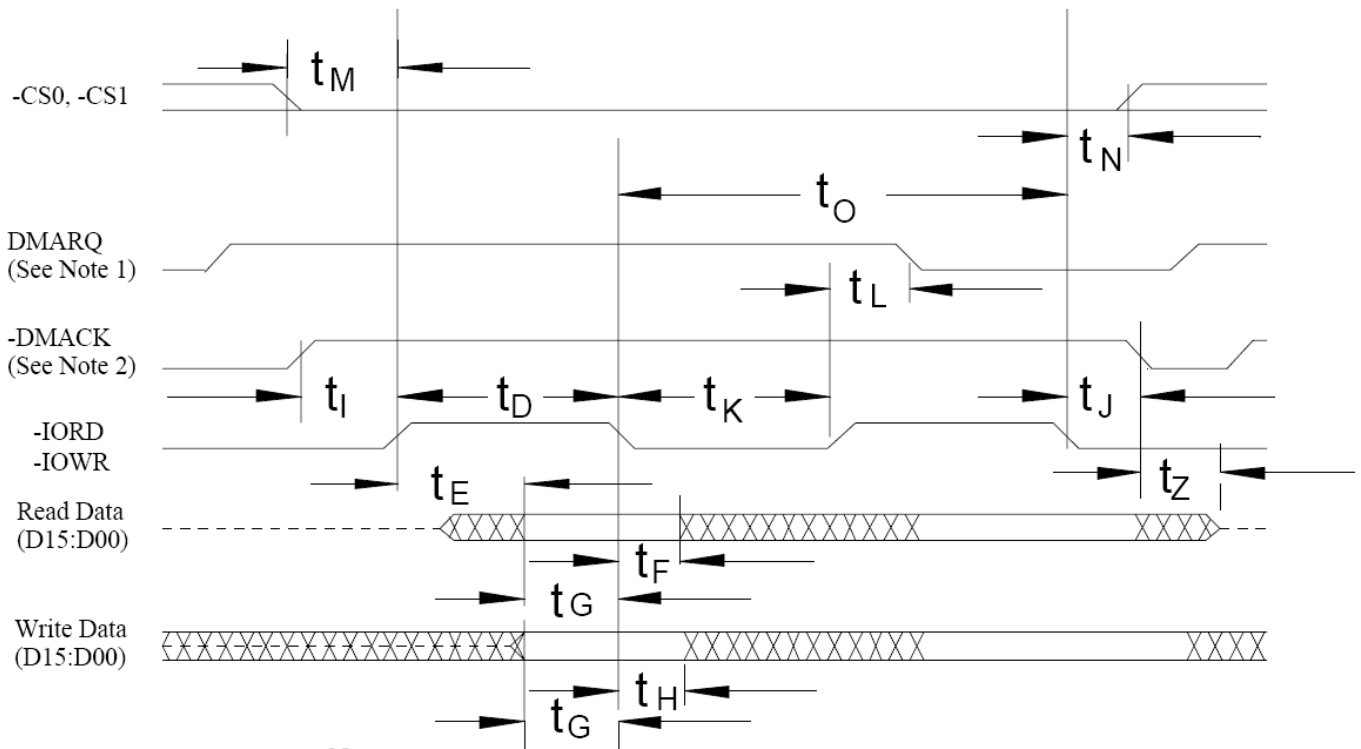
The timing diagram for true IDE DMA mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IOR , the -IOW and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 6: True IDE Multiword DMA mode Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Note
t_o	Cycle time (min)	480	150	120	1
t_D	$\text{-IOR}/\text{-IOW}$ asserted width (min)	215	80	70	1
t_E	-IOR data access (max)	150	60	50	
t_F	-IOR data hold(min)	5	5	5	
t_G	$\text{-IOR}/\text{-IOW}$ data setup(min)	100	30	20	
t_H	-IOW data hold(min)	20	15	10	
t_I	DMACK to $\text{-IOR}/\text{-IOW}$ setup (min)	0	0	0	
t_J	$\text{-IOR}/\text{-IOW}$ to -DMACK hold (min)	20	5	5	
t_{KR}	-IOR negated width (min)	50	50	25	1
t_{KW}	-IOW negated width (min)	215	50	25	1
t_{LR}	-IOR to DMARQ delay (max)	120	40	35	
t_{LW}	-IOW to DMARQ delay (max)	40	40	35	
t_M	CS(1:0) valid to -IOR / -IOW	50	30	25	
t_N	CS(1:0) hold	15	10	10	
t_Z	-DMACK	20	25	25	

Note:

1) t_o is the minimum total cycle time and t_D the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_o , t_D , t_{KR} , and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR} , and t_{KW} as needed to ensure that t_o is equal to or greater than the value reported in the device's identify device data.



Notes:

- (1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
- (2) This signal may be negated by the host to suspend the DMA transfer in progress.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Figure 9: True IDE Multiword DMA Read/Write Timing Diagram

4.5 True IDE Ultra DMA Mode Read/Write Timing Specification

4.5.1 Ultra DMA Data Transfers Timing

Table 7 and Table 8 define the timings associated with all phases of Ultra DMA bursts.

Table 7: Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		Measurement location (See Note 2)
	Min	Max	Min	Max	Min	Max	
t _{CYCTYP}	240		160		120		Sender
t _{CYC}	112		73		54		Note 3
t _{2CYC}	230		153		115		Sender
t _{DS}	15.0		10.0		7.0		Recipient
t _{DH}	5.0		5.0		5.0		Recipient
t _{DVS}	70.0		48.0		31.0		Sender
t _{DVH}	6.2		6.2		6.2		Sender
t _{CS}	15.0		10.0		7.0		Device
t _{CH}	5.0		5.0		5.0		Device
t _{CVS}	70.0		48.0		31.0		Host
t _{CVH}	6.2		6.2		6.2		Host
t _{ZFS}	0		0		0		Device
t _{DZFS}	70.0		48.0		31.0		Sender
t _{FS}		230		200		170	Device
t _{LI}	0	150	0	150	0	150	Note 4
t _{MLI}	20		20		20		Host
t _{UI}	0		0		0		Host
t _{AZ}		10		10		10	Note 5
t _{ZAG}	20		20		20		Host
t _{ZAD}	0		0		0		Device
t _{ENV}	20	70	20	70	20	70	Host
t _{RFS}		75		70		60	Sender
t _{RP}	160		125		100		Recipient
t _{IORDYZ}		20		20		20	Device
t _{ZIORDY}	0		0		0		Device
t _{ACK}	20		20		20		Host
t _{SS}	50		50		50		Sender

Note:

- 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5V.
- 2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and -DMARDY transitions are measured at the sender connector.
- 3) The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.
- 4) The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
- 5) The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a turnaround.
- 6) See the AX Timing requirements in Table 10: Ultra DMA AC Signal Requirements.

Table 8: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing	
t_{DZFS}	Time from data output released-to driving until the first transition of critical timing	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAG}	Minimum delay time required for output	
t_{ZAD}	Drives to assert or negate (from released)	
t_{ENV}	Envelope time(from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time(no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready to pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Note:

- 1) The parameters t_{UI} , t_{MLI} (in Figure 13: Ultra DMA Data-In Burst Device Termination Timing and Figure14: Ultra DMA Data-in Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
- 2) 80-conductor cabling shall be required in order to meet setup (t_{DS} , t_{CS}) and hold (t_{DH} , t_{CH}) times in modes greater than 3) Timing for t_{DVS} , t_{DVH} , t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
- 4) For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
- 5) The parameters t_{DS} and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

Table 9: Ultra DMA Sender and Recipient IC Timing Requirements

Name	Comments	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)	
		Min	Max	Min	Max	Min	Max
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note2)	14.7		9.7		6.8	
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)	4.8		4.8		4.8	
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)	72.9		50.9		33.9	
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)	9.0		9.0		9.0	

- Note:
- 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
 - 2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).
 - 3) The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Table 10: Ultra DMA AC Signal Requirements

Name	Comment	Min[V/ns]	Max[V/ns]	Notes
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

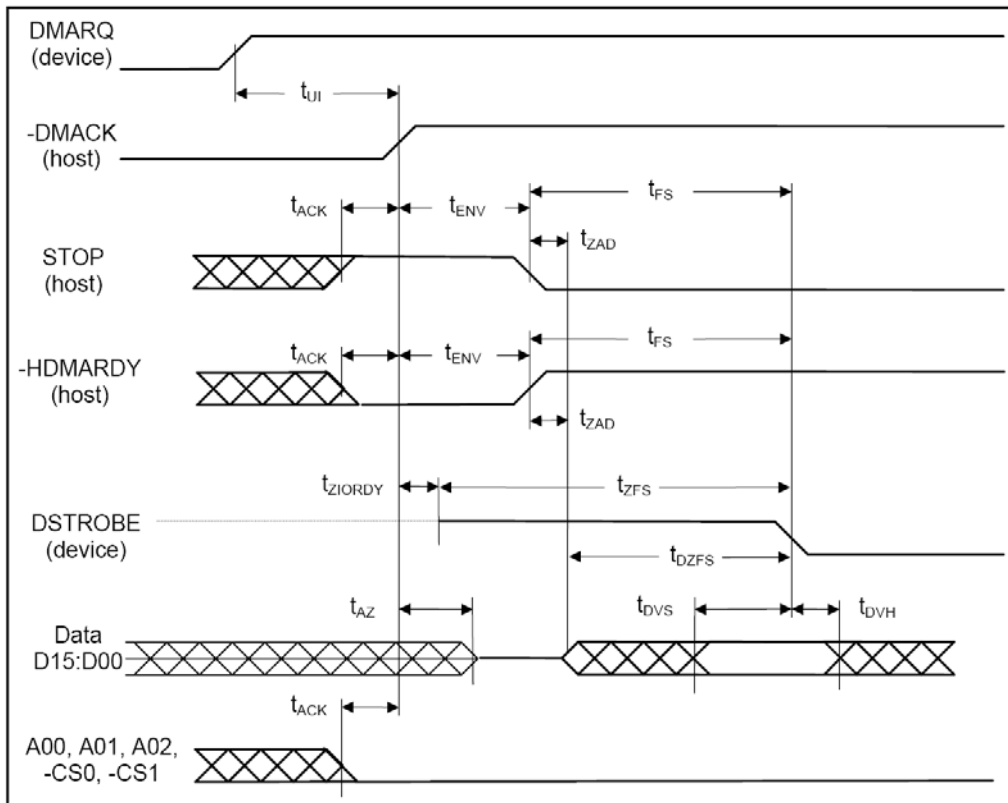
- Note:
- 1) The Sender shall be tested while driving an 18inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point in on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1pF, >100 Kohm, 1 GHz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

4.5.2 Initiating an Ultra DMA Data-In Burst

- a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 10: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.
- b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:
- c) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.
- d) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE .
- e) Steps(c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP .
- f) The host shall negate -HDMARDY .
- g) The host shall negate -CS0 , -CS1 , -DA2 , -DA1 , and DA0 . The host shall keep -CS0 , -CS1 , DA2 , DA1 , and DA0 negated until after negating -DMACK at the end of the burst.
- h) Steps(c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK . The host shall keep -DMACK asserted until the end of an Ultra DMA burst.
- i) The host shall release $\text{D}[15:00]$ within t_{AZ} after asserting -DMACK .
- j) The device may assert DSTROBE t_{ZIORDY} after the host has asserted -DMACK . Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA burst.
- k) The host shall negate STOP and assert -HDMARDY within t_{ENV} after asserting -DMACK . After negating STOP and asserting -HDMARDY , the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).
- l) The device shall drive $\text{D}[15:00]$ no sooner than t_{ZAD} after the host has asserted -DMACK , negated STOP , and asserted -HDMARDY .
- m) The device shall drive the first word of the data transfer onto $\text{D}[15:00]$. This step may occur when the device first drives $\text{D}[15:00]$ in step (j).
- n) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted -HDMARDY . The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto $\text{D}[15:00]$.



Notes: The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted.

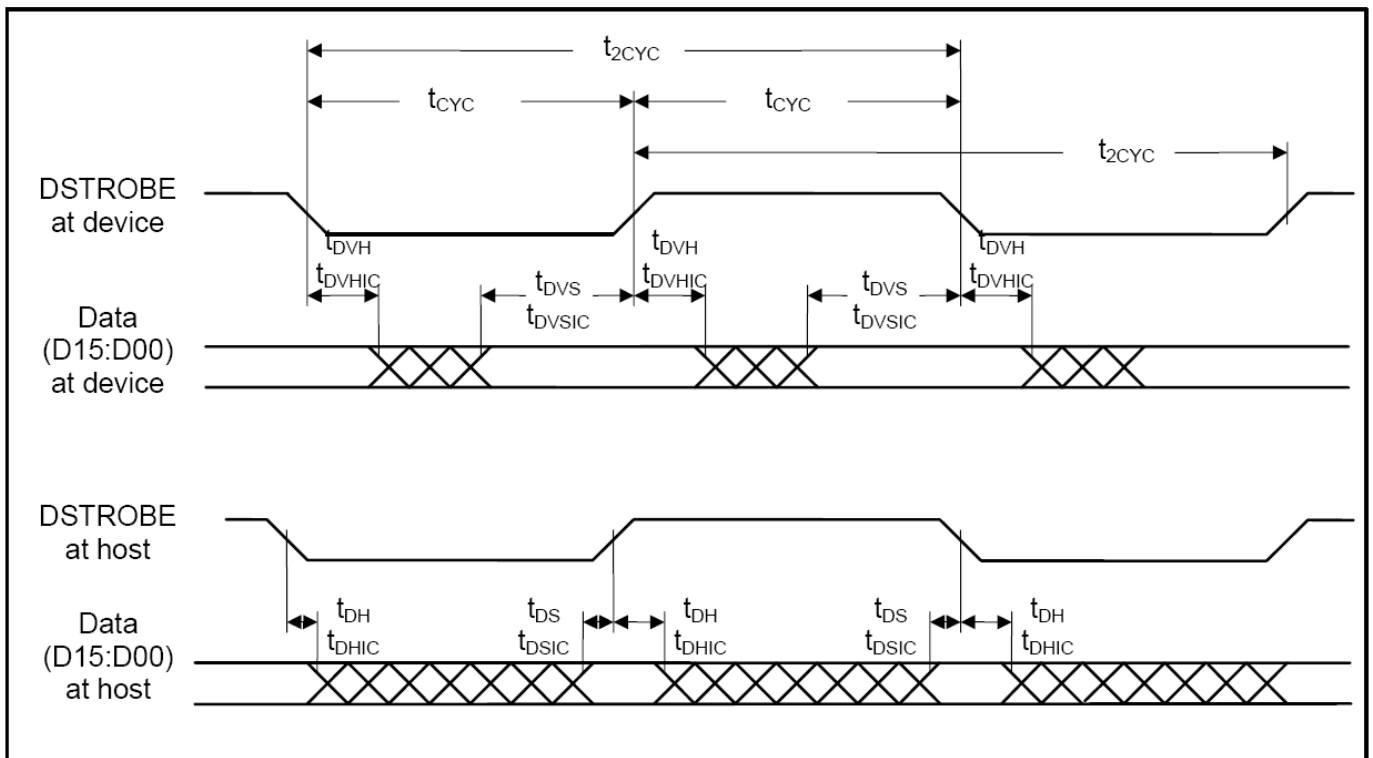
Figure 10: Ultra DMA Data-In Burst Initiation Timing

4.5.3 Sustaining an Ultra DMA data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 11: Sustained Ultra DMA Data-In Burst Timing. The timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The device shall drive a data word onto D[15:00].
- b) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D [15:00]. The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than $2t_{CYC}$ for the selected Ultra DMA mode.
- c) The device shall not change the state of D[15:00] until at least t_{DVH} after generating a DSTROBE edge to latch the data.
- d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.



Notes: **D[15:00]** and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

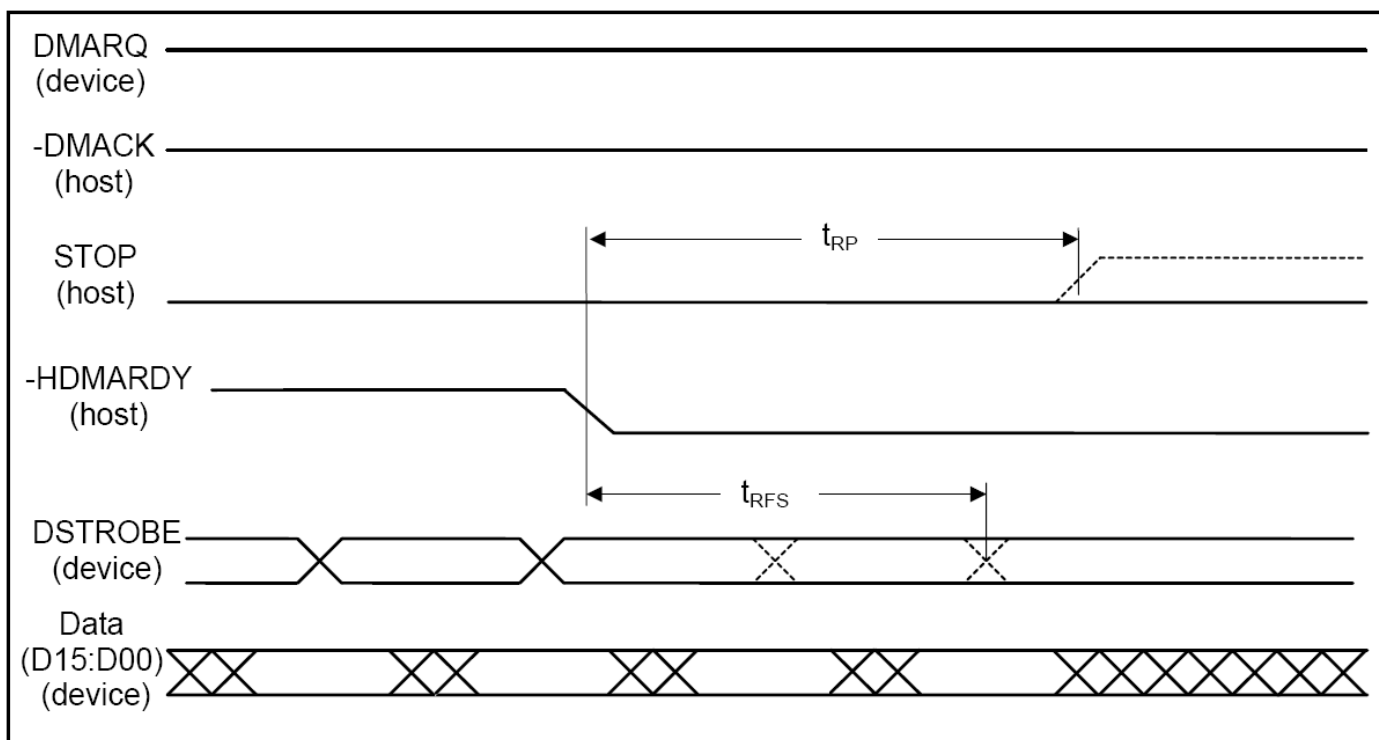
Figure 11: Sustained Ultra DMA Data-In Burst

4.5.4 Host Pausing an Ultra DMA Data-In Burst

The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in Figure 12: Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall pause an Ultra DMA burst by negating -HDMARDY.
- c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating -HDMARDY.
- d) If the host negates -HDMARDY within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates -HDMARDY greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
- e) The host shall resume an Ultra DMA burst by asserting -HDMARDY.



Notes:

- 1) The host may assert STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after -HDMARDY is negated.
- 2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

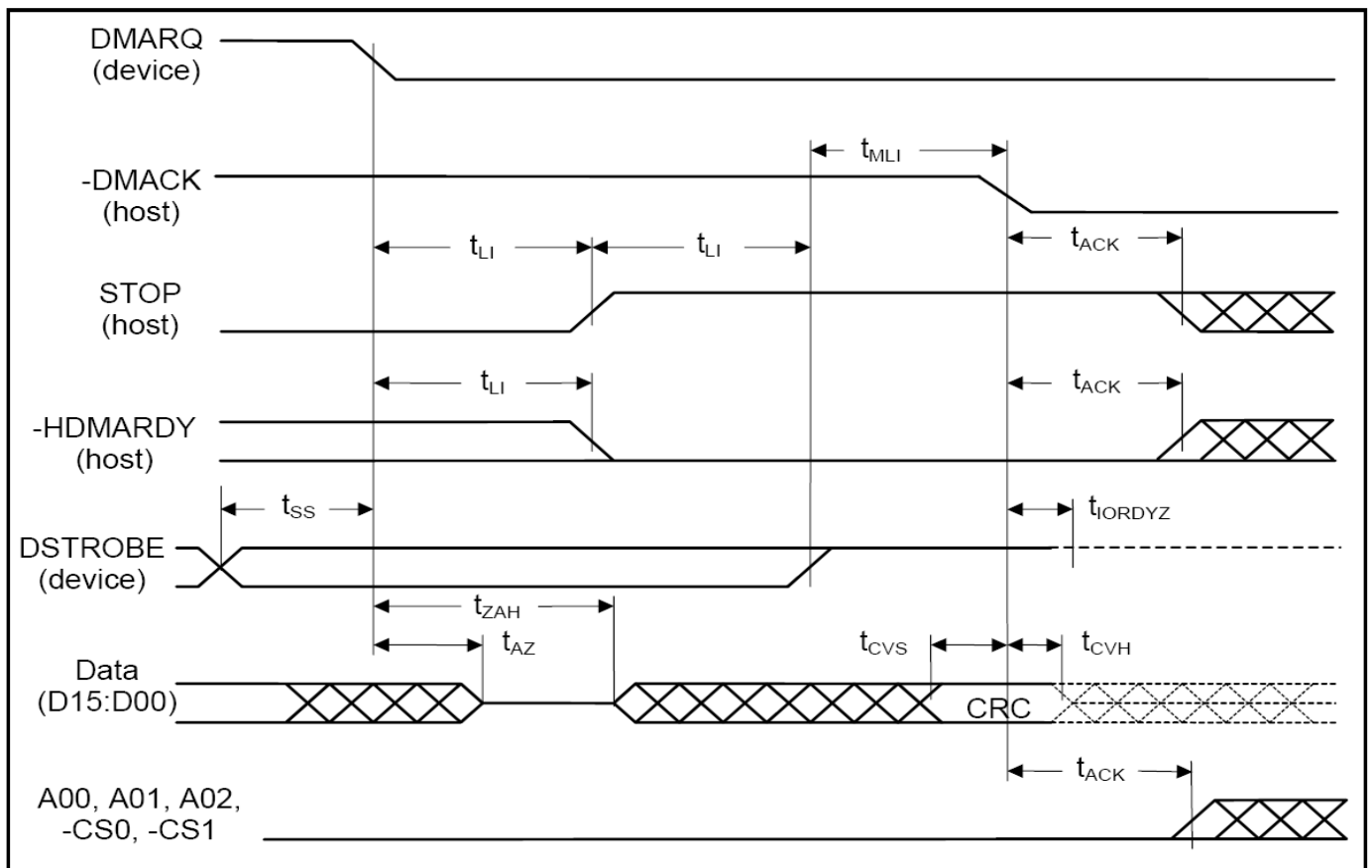
Figure 12: Ultra DMA Data-In Burst Host Pause Timing

4.5.5 Device Terminating an Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 13: Ultra DMA Data-In Burst Device Termination Timing. The timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.
- c) NOTE - The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate -HDMARDY and wait t_{RP} before asserting STOP.
- d) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

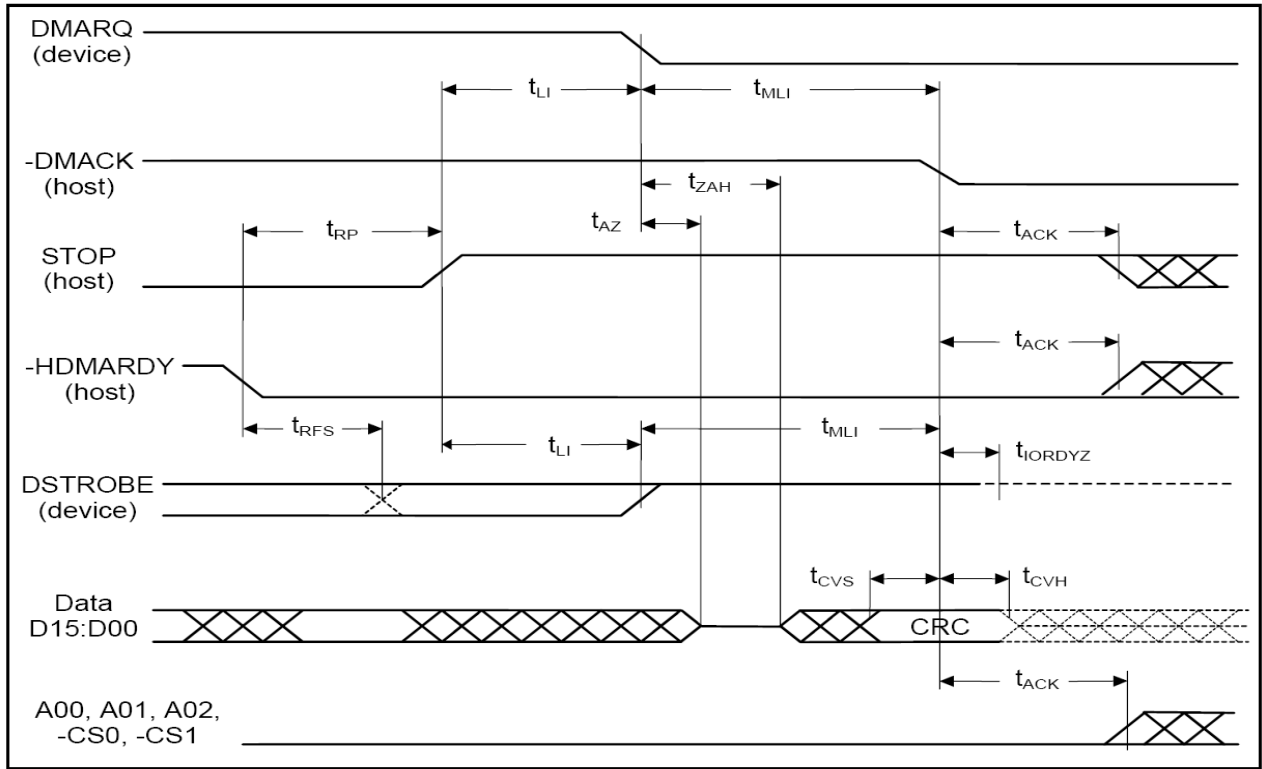
Figure 13: Ultra DMA Data-In Burst Device Termination Timing

4.5.6 Host Terminating an Ultra DMA Data-In Burst

The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 14: Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
- b) The host shall initiate Ultra DMA burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA burst is terminated.
- c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating -HDMARDY.
- d) If the host negates -HDMARDY within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
- e) The host shall assert STOP no sooner than t_{RP} after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- h) The device shall release D[15:00] no later than t_{AZ} after negating DMARQ.
- i) The host shall drive DD D[15:00] no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation.
- j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00].
- k) The host shall negate -DMACK no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated -HDMARDY, and no sooner than t_{DVS} after the host places the result of its CRC calculation on D[15:00].
- l) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
- m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred.
- n) The device shall release DSTROBE within t_{IORDYZ} after the host negates -DMACK.
- o) The host shall neither negate STOP nor assert -HDMARDY until at least t_{ACK} after the host has negated -DMACK.
- p) The host shall not assert -IORD, -CS0, -CS1, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated..

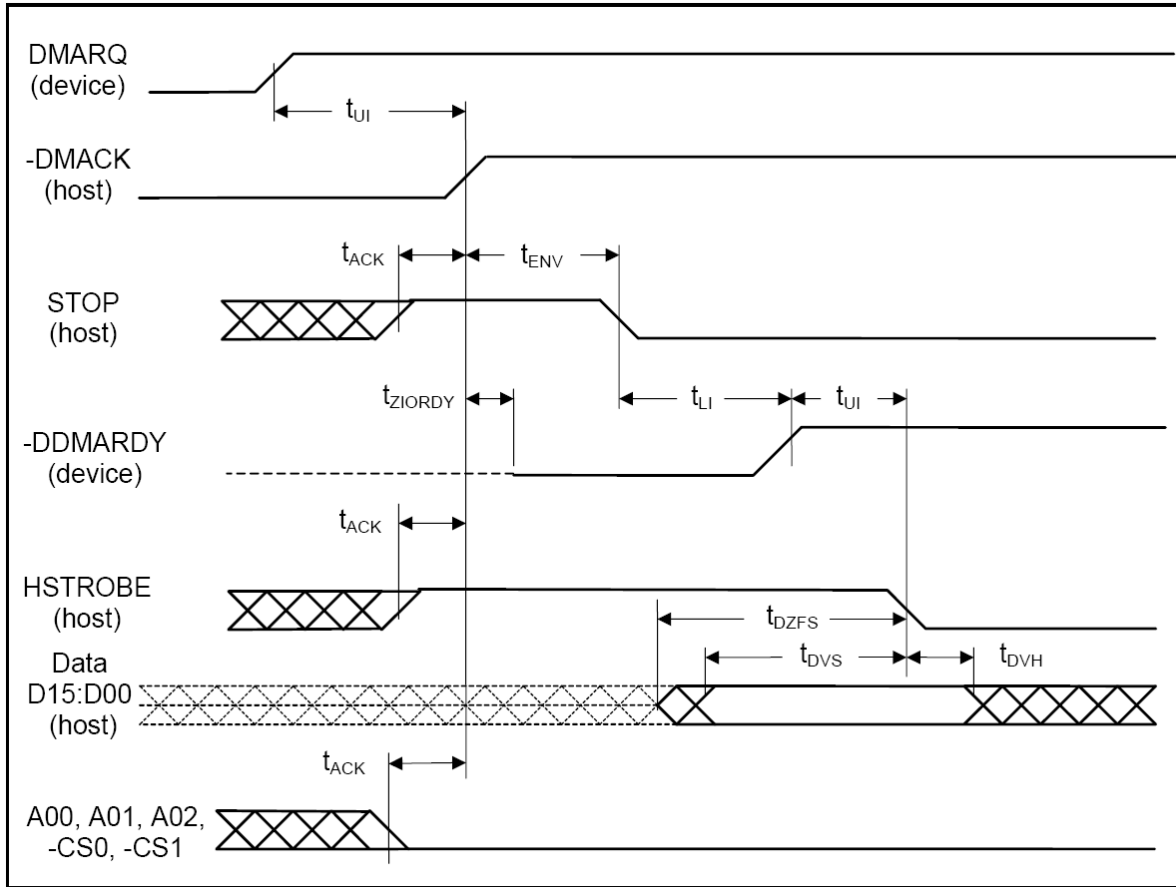
Figure 14: Ultra DMA Data-In Burst Host Termination Timing

4.5.7 Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 15: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.
- b) The device shall assert DMARQ to initiate an Ultra DMA burst.
- c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP .
- d) The host shall assert HSTROBE .
- e) The host shall negate -CS0 , -CS1 , DA2 , DA1 , and DA0 . The host shall keep -CS0 , -CS1 , DA2 , DA1 , and DA0 negated until after negating -DMACK at the end of the burst.
- f) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK . The host shall keep -DMACK asserted until the end of an Ultra DMA burst.
- g) The device may negate -DDMARDY t_{ZIORDY} after the host has asserted -DMACK . Once the device has negated -DDMARDY , the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.
- h) The host shall negate STOP within t_{ENV} after asserting -DMACK . The host shall not assert STOP until after the first negation of HSTROBE .
- i) The device shall assert -DDMARDY within t_{LI} after the host has negated STOP . After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.
- j) The host shall drive the first word of the data transfer onto $\text{D}[15:00]$. This step may occur any time during Ultra DMA burst initiation.
- k) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} after the device has asserted -DDMARDY . The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto $\text{D}[15:00]$.



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

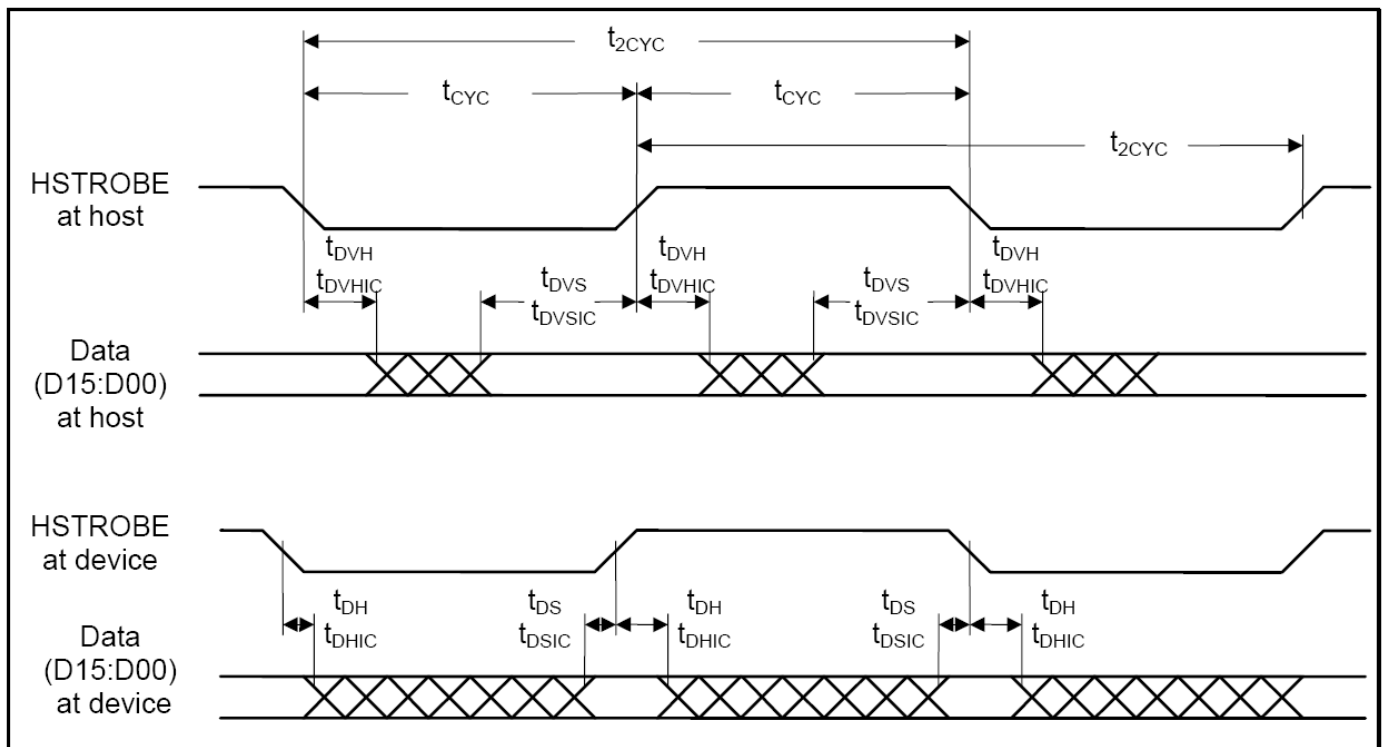
Figure 15: Ultra DMA Data-Out Burst Initiation Timing

4.5.8 Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 16: Sustained Ultra DMA Data-Out Burst Timing. The associated timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall drive a data word onto D [15:00].
- b) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D [15:00]. The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than $2t_{CYC}$ for the selected Ultra DMA mode.
- c) The host shall not change the state of D[15:00] until at least t_{DVH} after generating an HSTROBE edge to latch the data.
- d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.



Note: Data (D15:D00) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

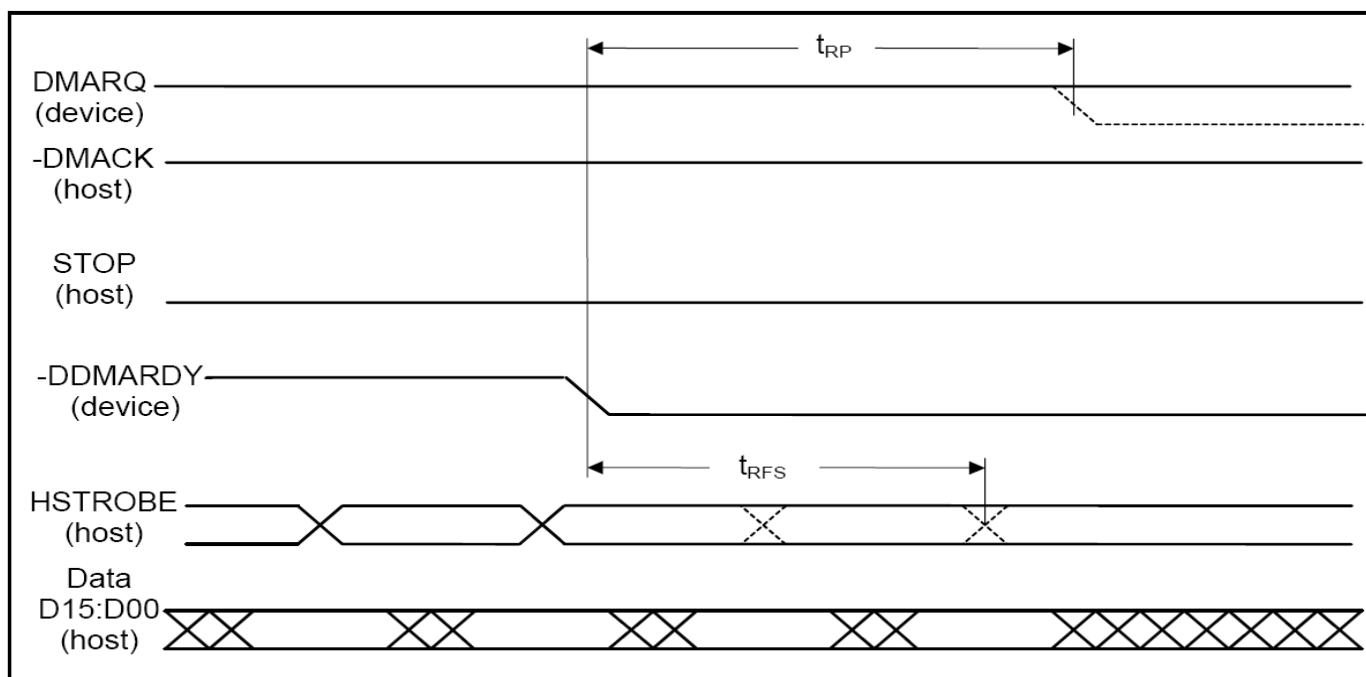
Figure 16: Sustained Ultra DMA Data-Out Burst Timing

4.5.9 Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in Figure 17: Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall pause an Ultra DMA burst by negating -DDMARDY.
- c) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating -DDMARDY.
- d) If the device negates -DDMARDY within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
- e) The device shall resume an Ultra DMA burst by asserting -DDMARDY.



Notes: 1) The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than t_{RP} after -DDMARDY is negated.
 2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

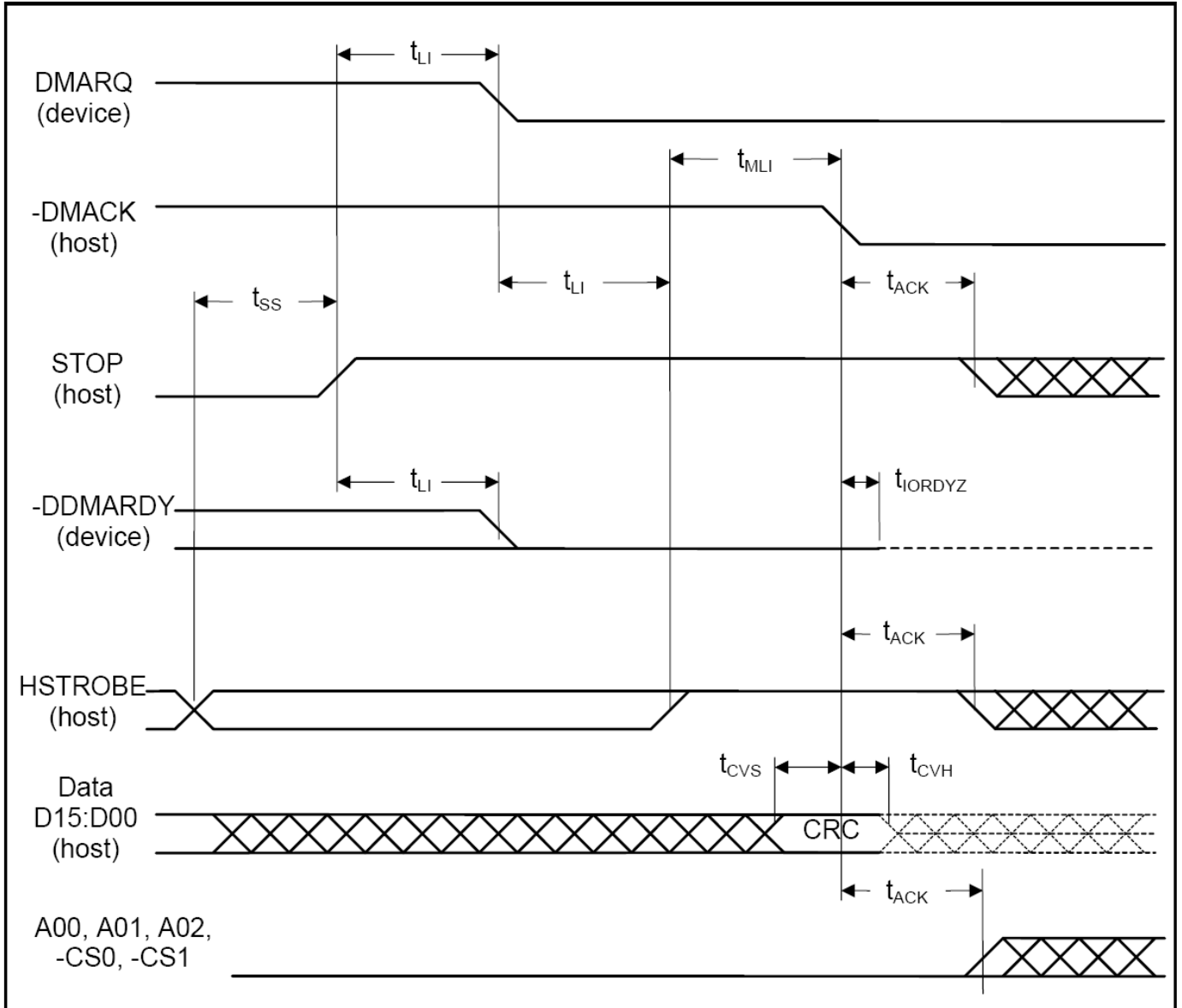
Figure 17: Ultra DMA Data-Out Burst Device Pause Timing

4.5.10 Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in Figure 18: Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
- b) The device shall initiate Ultra DMA burst termination by negating -DDMARDY.
- c) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating -DDMARDY.
- d) If the device negates -DDMARDY within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
- e) The device shall negate DMARQ no sooner than t_{RP} after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- f) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- g) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- h) The host shall place the result of its CRC calculation on D[15:00]
- i) The host shall negate -DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].
- j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
- k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a mis-compare error occurs during one or more Ultra DMA bursts for any one command,



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

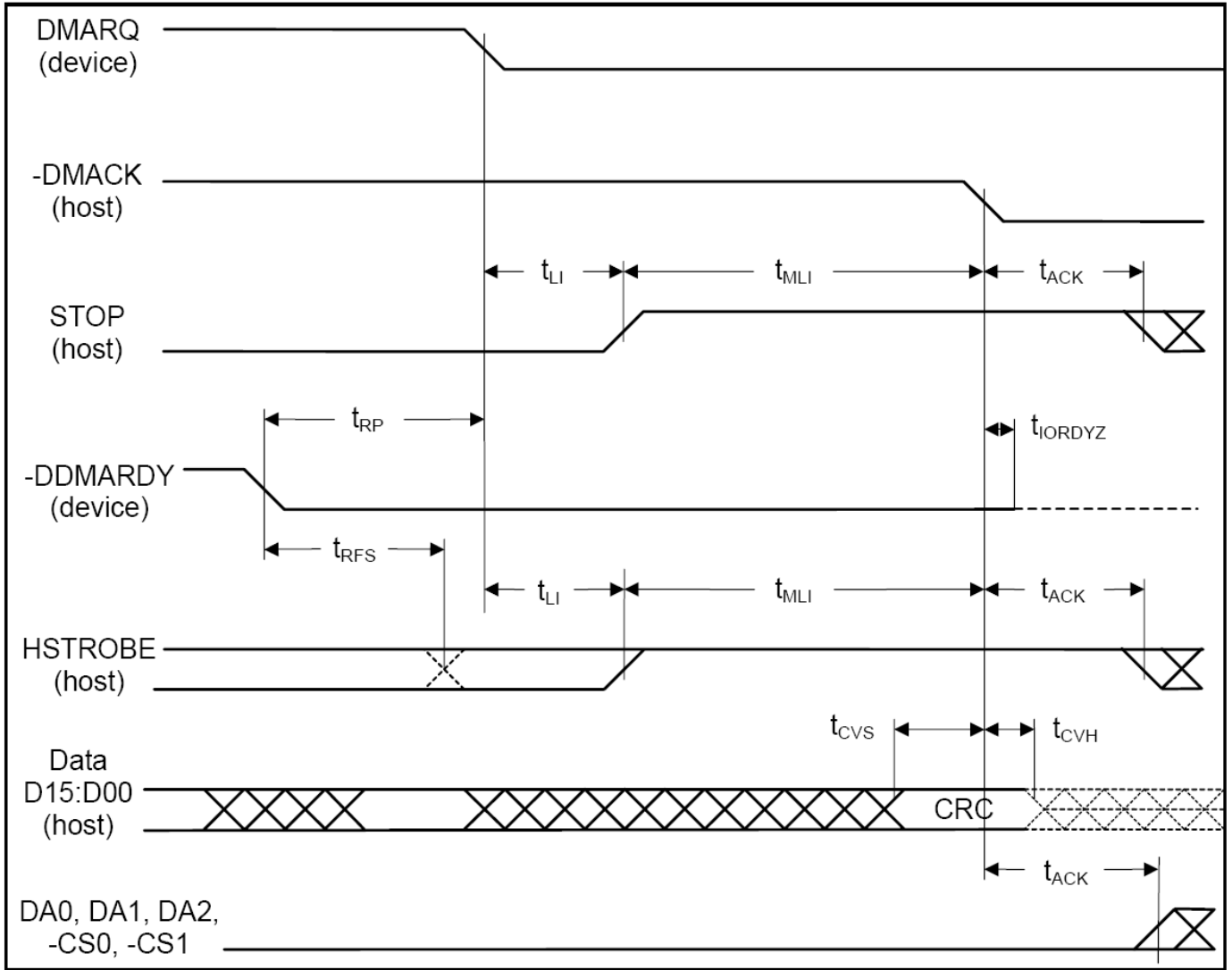
Figure 18: Ultra DMA Data-Out Burst Device Termination Timing

4.5.11 Host Terminating an Ultra DMA Data-Out Burst

Termination of an Ultra DMA Data-Out burst by the host is shown in Figure 19: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Table 7: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Table 8: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

- a) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.
- b) The host shall assert STOP no sooner than t_{SS} after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
- c) The device shall negate DMARQ within t_{LI} after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
- d) The device shall negate -DDMARDY within t_{LI} after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA burst termination is complete.
- e) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
- f) The host shall place the result of its CRC calculation on D[15:00].
- g) The host shall negate -DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].
- h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
- i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a mis-compare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.
- j) The device shall release -DDMARDY within t_{IORDYZ} after the host has negated -DMACK.
- k) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating -DMACK.
- l) The host shall not assert -IOWR, -CS0, -CS1, DA2, DA1, or DA0 until at least t_{ACK} after negating -DMACK.



Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 19: Ultra DMA Data-Out Burst Host Termination Timing

4.6 True IDE Mode I/O Transfer Function

Table 11: True IDE mode I/O Function

Function Codes	-CS1	-CS0	A0-A2	-DMACK	-IORD	-IOWR	D15-D8	D7-D0
Invalid Modes	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined in	Undefined in
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined in	Undefined in
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte in	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte in	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 2		Odd-Byte in	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 3		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address ¹	L	H	7h	H	L	H	High Z	Data Out

Notes:

- 1) Implemented for backward compatibility. Bit D7 of the register shall remain High Z to prevent conflict with any floppy disk controller at the same address. The host software should not rely on the contents of this register.
- 2) In Ultra DMA Data Register Write mode the signals -IORD, -IOWR and IORDY are redefined and used as follows: -IORD as HSTROBE, -IOWR as STOP and IORDY as -DDMARDY. Data transfers with each edge of HSTROBE. See Section 6.11: True IDE Ultra DMA Mode Read/Write Timing Specification and Table 5: Signal Description for complete information.
- 3) In Ultra DMA Data Register Read mode the signals -IORD, -IOWR and IORDY are redefined and used as follows: -IORD as -HDMARDY H, -IOWR as STOP and IORDY as DSTROBE. Data transfers with each edge of DSTROBE.

5. Installation

5.1 Installation

- For Installation of DiskOnModule to your system, please follow up below steps;
 1. Make sure your computer is turned off before you open the case.
 2. Plug the DiskOnModule carefully into the IDE slot on your computer or host adapter.
 3. Connect the power cable of the DiskOnModule.
 4. Check cable connections and DiskOnModule is firm enough.

5.2 Partition

- For DOS Operating System :

- To partition your new DiskOnModule for example use Microsoft DOS program:

1. Insert a bootable DOS diskette into your diskette drive and restart your computer.
2. Insert a DOS program diskette that contains the **FDISK.EXE** and **FORMAT.COM** programs into your diskette drive. Use the same DOS version that is on your bootable diskette. At the A: prompt, type **FDISK** and press **ENTER**.
3. Select "Create DOS partition or logical DOS drive" by pressing **1**. Then press **ENTER**.
4. Select "**Create primary DOS partition**" by pressing **1** again. Then press **ENTER**. Create your first drive partition. If you are creating a partition that will be used to boot your computer (drive C), make sure that the partition is marked active.
5. Create an extended partition and additional logical drives as necessary, until all the space on your new hard drive has been partitioned.
6. When the partitioning is complete, **FDISK** reboots your computer.

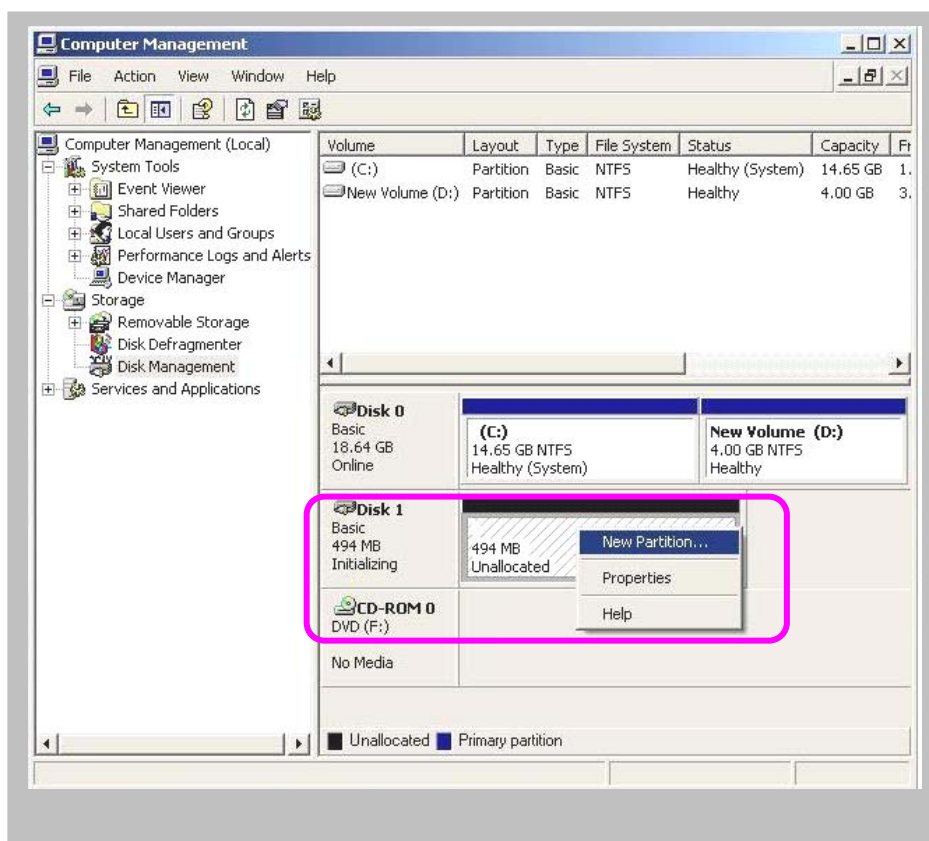
※ Note: Make sure to use the correct drive letters so that you do not format a drive that already contains data.

8. At the A: prompt, type **format c:/s**, where c is the letter of your first new partition, Repeat the format process for all the new partitions you have created.
9. After you format your DiskOnModule, it is ready to use.

For Windows Operating System :

- To partition your new DiskOnModule, for example use Microsoft WindowsXP and WindowsXP embedded system :

1. Into your windows system. You can Click the 『 Start 』 → 『 Control Panel 』 → 『 Administrative Tools 』 → 『 Computer Management 』 then select 『 Storage 』 → 『 Disk Manager 』 to setup the partition.



5.3 Format

- For DOS Operating System :

- Before you format or partition your new DiskOnModule, you must configure your computer's BIOS so that the computer can recognize your new DiskOnModule.

1. Turn your computer on. As your computer start up, watch the screen for a message describing how to run the system setup program (sometimes called BIOS or CMOS setup). This is usually done by pressing a special key, such as DELETE, ESC, or F1, during startup. See your computer manual for details. Press the appropriate key to run the system setup program.

2. If your BIOS provides automatic drive detection (an "AUTO" drive type), select this option. (If you use Normal/CHS mode to partition your DOM, you can get the maximum formatted capacity.)

This allows your computer to configure itself automatically for your new DiskOnModule.

If your BIOS does not provide automatic drive detection, select "User-defined" drive setting and enter the CHS values from the table.

BIOS Settings (see specification)

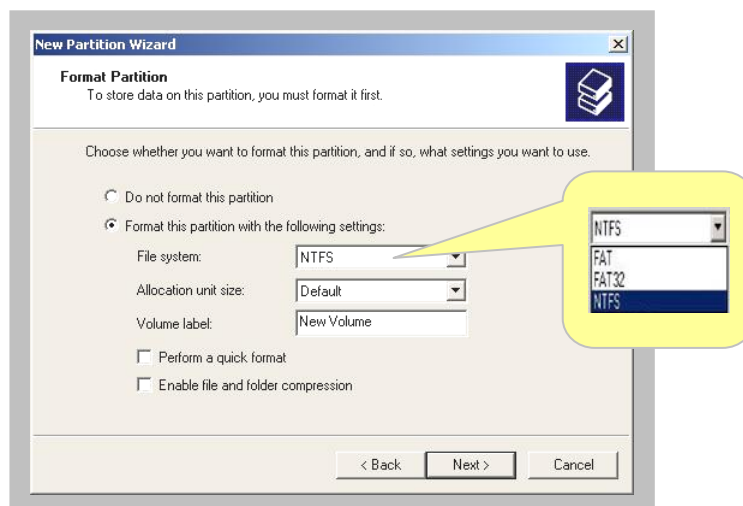
Capacity	Cylinders	Heads	Sectors	(unformatted)
----------	-----------	-------	---------	---------------

3. Save the settings and exit the System Setup program.
(Your computer will be automatically rebooted.)

For Windows Operating System :

- To partition your new DOM, for example use Microsoft WindowsXP and WindowsXP embedded system :

1. Click the 『 Start 』 → 『 Control Panel 』 → 『 Administrative Tools 』 → 『 Computer Management 』 then select 『 Storage 』 → 『 Disk Manager 』 to setup the file format.
2. Select “FAT or NTFS” format for user.



6. Troubleshooting

6.1 BIOS can not identify DiskOnModule

- a. Check Power Cable Status
- b. Check Connector status
- c. Check the Power Voltage (5V or 3.3V)

6.2 DOM can not boot the system

- a. Check BIOS setting
- b. Reinstall your system

Notice Please contact your closest CSS office for verifying your other troubles.

7. Ordering Information

Table 12: DiskOnModule Ordering Information

P/N	Capacity (Max)
DJ0128M ^{*1} 46R ^{*2} F ^{*3} 0	4GB

^{*1} : 128M:128MB, 256M:256MB, 512M:512MB, 010G:1GB, 020G:2GB, 040G:4GB

^{*2} : R: Industrial type T: Wide Temperature type

^{*3} : Flash Density
E:64MB, F:128MB, I:256MB, L:512MB, N:1GB, P:2GB

^{*4} : DJ0128M46RF0(WP): With Write Protect Switch
DJ0128M46RF0 : Without Write Protect Switch

8. Contact Information

CoreSolid Storage Corporation, a TDK-PQI storage business company, specializes in the design and marketing of SSD, DOM, and Industry CF products.



For further information, please reach us at the following contact information:

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- Sales: sales@coresolid-storage.com
- Customer Service: support.jp@coresolid-storage.com